PRELIMINARY

51C256H
HIGH PERFORMANCE RIPPLEMODE™ 256K × 1 CHMOS DYNAMIC RAM

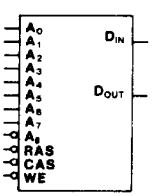
	51C256H-10†	51C256H-12	51C256H-15	51C256H-20
Maximum Access Time (ns)	100	120	150	200
Maximum Column Address Access Time (ns)	40	50	65	85
Ripplemode Cycle Time (ns)	50	60	75	95

- **Ripplemode™ Operation**
  - **Continuous data rate up to 20 MHz**
  - **Random access within a row**
  - **Flow through column latch for pipelining**
- **Low Operating Power — 50 mA**
- **Low Input/Output Capacitance**
- **Fast "Usable Speed"**
  - **t_{RC} = 170 ns**
  - **t_{CAC} = 25 ns**
  - **t_{RCD} = 30 ns min./75 ns max.**
- **Fully TTL Compatible**
- **High Reliability Plastic — 16 Pin DIP, 18 Pin PLCC**

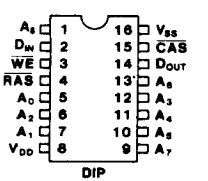
The Intel 51C256H is a high speed 262,144 × 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C256H offers features not provided by an NMOS dynamic RAM: Ripplemode for high data bandwidth and fast usable speed. All inputs and outputs are TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

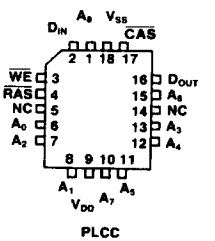
Ripplemode operation allows random or sequential access of up to 512 bits within a row, with cycle times as fast as 50 ns. Because of static column circuitry, the $\overline{CAS}$ clock is no longer in the critical timing path. The flow through column latch allows address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the 51C256H ideally suited for cache based mainframe and mini computers, graphics, digital signal processing, and high performance microprocessor systems.

LOGIC SYMBOL



PIN CONFIGURATION





PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_8	ADDRESS INPUTS
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

† Available 1986

JUNE 1985
Order Number: 280030-003

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature .. Plastic −55°C to +125°C
Voltage on Any Pin except D_{OUT}
Relative to V_{SS} ..... −1.0V to 7.5V
Voltage on D_{OUT}
Relative to V_{SS} ..... −1.0V to V_{DD} + 1V
Data Out Current ..... 50 mA
Power Dissipation 1.0W

†COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1]

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C256H			Unit	Test Conditions	Notes
		Min.	Typ.[2]	Max.			
I_{DD1}	V_{DD} Supply Current, Operating			80	mA	$t_{RC} = t_{RC(min)}$, for -10 specification	3, 4
				75	mA	$t_{RC} = t_{RC(min)}$, for -12 specification	
			48	60	mA	$t_{RC} = t_{RC(min)}$, for -15 specification	
			35	50	mA	$t_{RC} = t_{RC(min)}$, for -20 specification	
I_{DD2}	V_{DD} Supply Current, TTL Standby		1	4	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, all other inputs and output ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh			80	mA	$t_{RC} = t_{RC(min)}$, for -10 specification	4
				75	mA	$t_{RC} = t_{RC(min)}$, for -12 specification	
			45	60	mA	$t_{RC} = t_{RC(min)}$, for -15 specification	
			35	50	mA	$t_{RC} = t_{RC(min)}$, for -20 specification	
I_{DD4}	V_{DD} Supply Current, Ripplemode			80	mA	$t_{PC} = t_{PC(min)}$, for -10 specification	3,4
				75	mA	$t_{PC} = t_{PC(min)}$, for -12 specification	
			22	60	mA	$t_{PC} = t_{PC(min)}$, for -15 specification	
			18	50	mA	$t_{PC} = t_{PC(min)}$, for -20 specification	
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		3	6	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IL}, all other inputs and outputs ≥ V_{SS}	3
$\lvert I_{LI} \rvert$	Input Load Current (any pin)			10	μA	$V_{IN} = V_{SS}$ to V_{DD}	
$\lvert I_{LO} \rvert$	Output Leakage Current for High Impedance State			10	μA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, $D_{OUT} = V_{SS}$ to V_{DD}	
V_{IL}	Input Low Voltage (all inputs)	−0.3		0.8	V		5
V_{IH}	Input High Voltage (all inputs)	2.4		V_{DD} + 1	V		5
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	6
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −5 mA	6

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are at T_A = 25°C and V_{DD} = +5V.
3. I_{DD} is dependent on output loading when the device output is selected. Specified $I_{DD(max)}$ is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified $I_{DD(max)}$ is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Ripplemode.
5. Specified $V_{IL(min)}$ is steady state operation. During transitions, V_{IL} may undershoot to −1.0 V for periods not to exceed 20 ns. All A.C. parameters are measured with $V_{IL(min)} \geq V_{SS}$ and $V_{IH(max)} \leq V_{DD}$.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address D_{IN}	4	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	3	5	pF
C_{OUT}	D_{OUT}	4	6	pF

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable Hewlett Packard capacitance meter.

A.C. CHARACTERISTICS[1,2,3]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

No.	Symbol	Parameter	51C256H-10		51C256H-12		51C256H-15		51C256H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	150	75000	200	75000	ns	
2	t_{RC}	Random Read or Write Cycle Time	170		200		245		315		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	60		70		85		105		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	100		120		150		200		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	25	75000	30	75000	30	75000	35	75000	ns	
6	t_{WRP}	$\overline{Write\ Enable}$ To $\overline{RAS}$ Precharge Time	10		10		10		10		ns	
7	t_{RWH}	$\overline{RAS}$ To $\overline{Write\ Enable}$ Hold Time	15		15		20		25		ns	
8	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RAH}	Row Address Hold Time	20		20		20		25		ns	
10	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
11	t_{CRP}	$\overline{CAS}$ To $\overline{RAS}$ Precharge Time	10		10		10		10		ns	
12	t_{RCD}	$\overline{RAS}$ To $\overline{CAS}$ Delay	30	75	30	90	30	120	35	165	ns	4
13	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
14	t_{CAH}	Column Address Hold Time	15		20		20		25		ns	
15	t_{AR}	Column Address Hold Time From $\overline{RAS}$	50		60		65		70		ns	
	t_{REF}	Time Between Refresh		4		4		4		4	ms	
	t_T	Transition Time (Rise and Fall)	1	25	1	25	1	25	1	25	ns	5
16	t_{ON}	Output Buffer Turn On Delay	0		0		0		0		ns	
17	t_{OFF}	Output Buffer Turn Off Delay		20		25		25		30	ns	

NOTES:

1. All voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).
3. A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, $V_{IL(min)} \geq V_{SS}$ and $V_{IH(max)} \leq V_{DD}$.
4. t_{RCD} is specified for reference only. If $t_{RCD} \geq t_{RCD(max)}$, the t_{RAC} will increase by the amount that t_{RCD} exceeds $t_{RCD(max)}$.
5. t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

A.C. CHARACTERISTICS (Continued)

Read Cycle

No.	Symbol	Parameter	51C256H-10		51C256H-12		51C256H-15		51C256H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
18	t_{RAC}	Access Time From $\overline{RAS}$		100		120		150		200	ns	6
19	t_{CAC}	Access Time From $\overline{CAS}$		25		30		30		35	ns	7,8
20	t_{CAA}	Access Time From Column Address		40		50		65		85	ns	8
21	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		10		10		ns	
22	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
23	t_{CAR}	Column Address To $\overline{RAS}$ Setup Time	40		50		65		85		ns	
24	t_{RCH}	Read Command Hold Time Ref. To $\overline{CAS}$	5		5		5		5		ns	9
25	t_{RRH}	Read Command Hold Time Ref. To $\overline{RAS}$	10		10		10		10		ns	9

Write Cycle

No.	Symbol	Parameter	51C256H-10		51C256H-12		51C256H-15		51C256H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
26	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	25		30		30		35		ns	
27	t_{RWL}	Write Command To $\overline{RAS}$ Lead Time	25		30		30		35		ns	
28	t_{CWL}	Write Command To $\overline{CAS}$ Lead Time	25		30		30		35		ns	
29	t_{WP}	Write Command Pulse Width	15		20		25		30		ns	
30	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	10
31	t_{WCH}	Write Command Hold Time	20		25		30		35		ns	
32	t_{DS}	Data-In Setup Time	0		0		0		0		ns	
33	t_{DH}	Data-In Hold Time	20		25		25		30		ns	

NOTES:

6. Assumes that $t_{RCD} \leq t_{RCD(max)}$. If $t_{RCD} > t_{RCD(max)}$, then t_{RAC} will increase by the amount that t_{RCD} exceeds $t_{RCD(max)}$.
7. Assumes $t_{RCD} \geq t_{RCD(max)}$.
8. If $t_{ASC} < (t_{CAA(max)} - t_{CAC(max)} - t_T)$, then access time is defined by t_{CAA} rather than by t_{CAC}.
9. Either t_{RCH} or t_{RRH} must be satisfied.
10. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

280030-003

A.C. CHARACTERISTICS (Continued)

Read-Modify-Write Cycle[11]

No.	Symbol	Parameter	51C256H-10		51C256H-12		51C256H-15		51C256H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
34	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	200		235		280		355		ns	
35	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	130	75000	155	75000	185	75000	240	75000	ns	
36	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	55	75000	65	75000	65	75000	75	75000	ns	
37	t_{RWD}	$\overline{RAS}$ To $\overline{WE}$ Delay	100		120		150		200		ns	12
38	t_{CWD}	$\overline{CAS}$ To $\overline{WE}$ Delay	25		30		30		35		ns	12
39	t_{AWD}	Column Address To $\overline{WE}$ Delay	40		50		65		85		ns	12

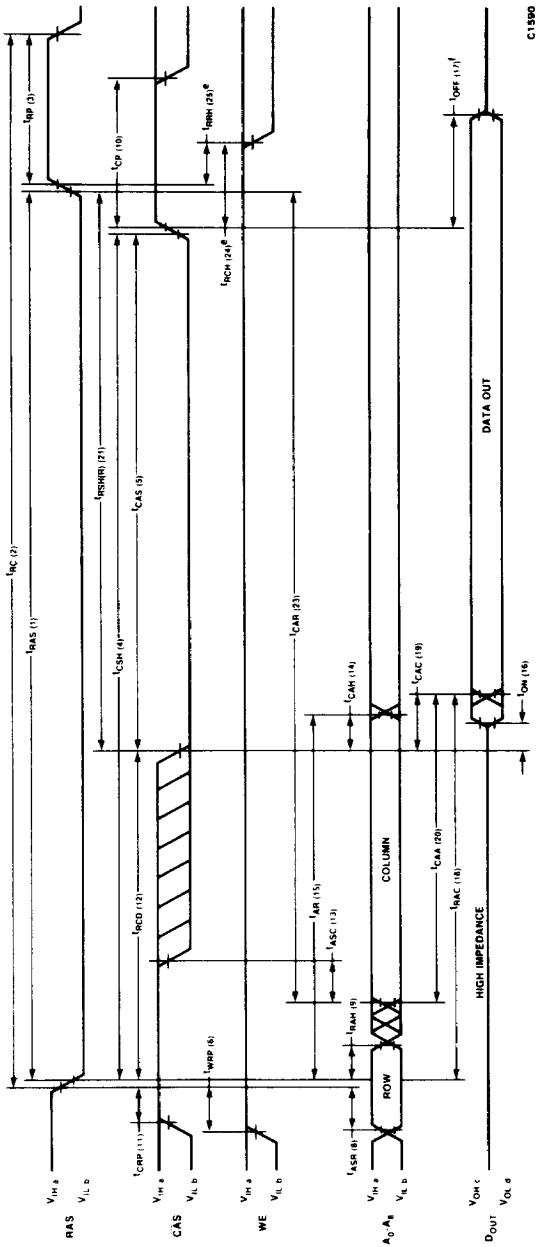
Ripplemode Cycle[13]

No.	Symbol	Parameter	51C256H-10		51C256H-12		51C256H-15		51C256H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
40	t_{CAP}	Access Time From Column Precharge		45		55		70		90	ns	14
41	t_{PC}	Ripplemode Read Or Write Cycle	50		60		75		95		ns	14
42	t_{PCM}	Ripplemode RMW Cycle Time	80		95		110		135		ns	

NOTES:

11. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
12. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is a $\overline{CAS}$ controlled write cycle and the data out pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data is indeterminate.
13. All previously specified A.C. Characteristics are applicable.
14. Access time is determined by the longer of t_{CAA} or t_{CAC} or t_{CAP}.

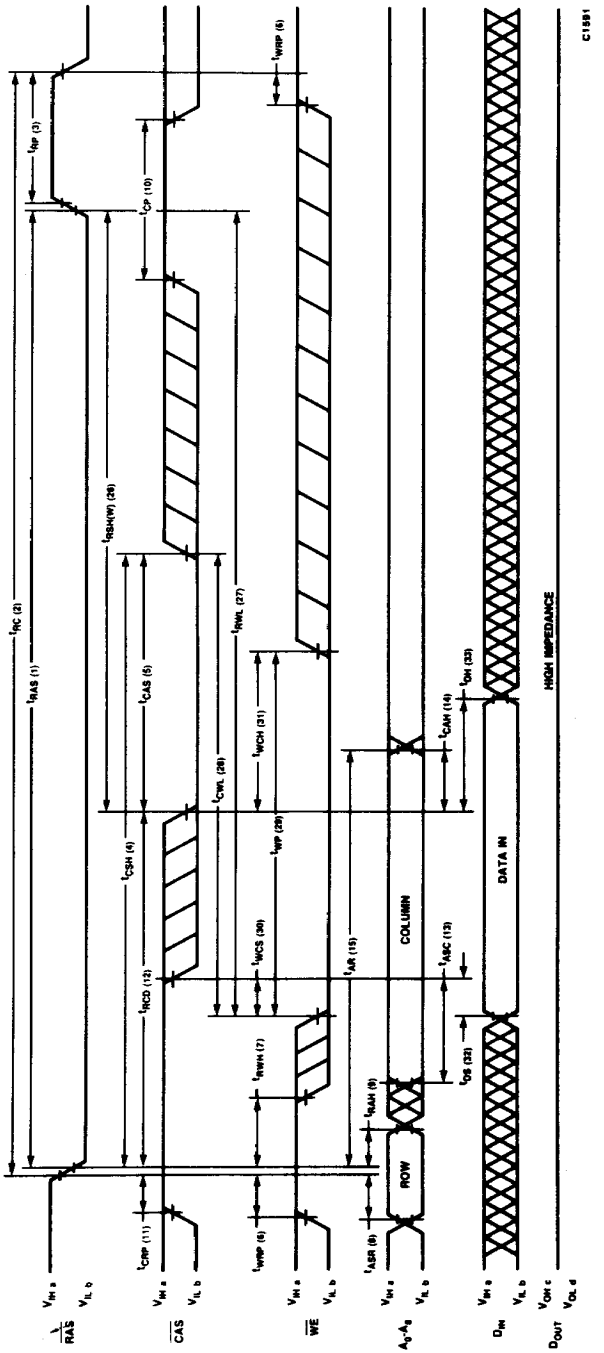
WAVEFORMS
Read Cycle



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. Either t_{RCH} or t_{RRH} must be satisfied.
f. I_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

280030-003

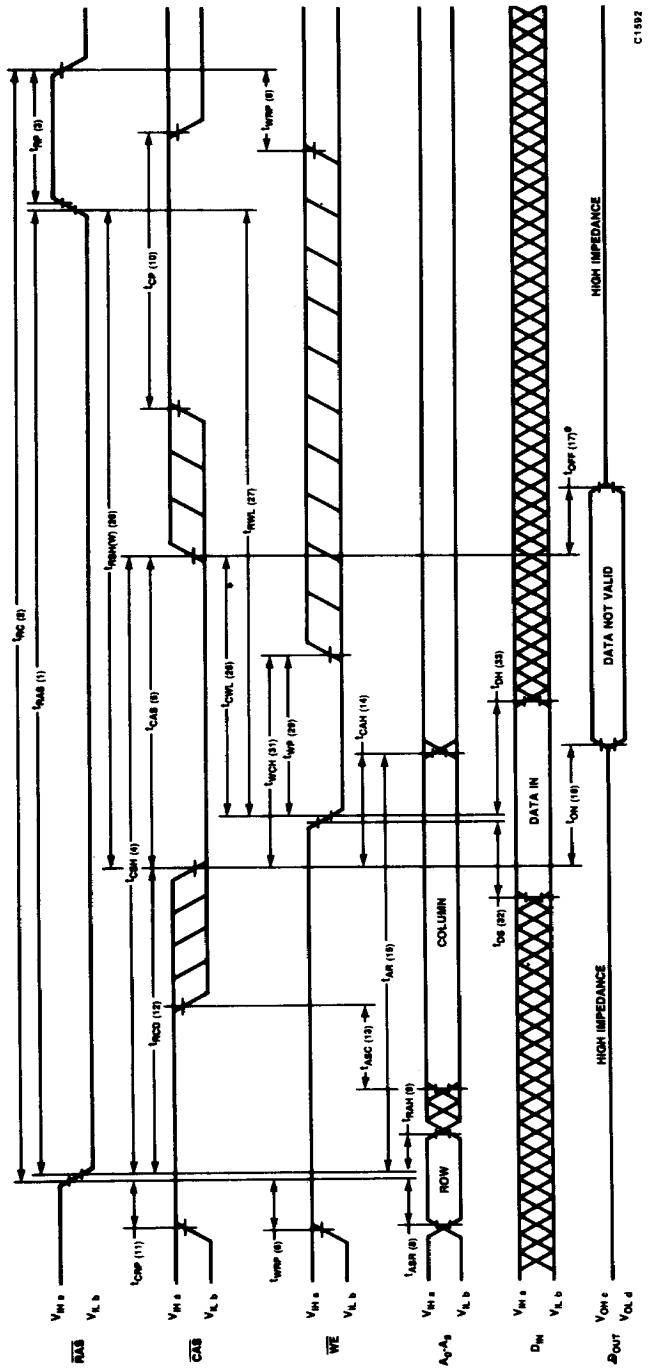
WAVEFORMS (Cont.)
Write Cycle ($\overline{CAS}$ Controlled)[e]



NOTES: a.b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c.d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ latches column address and data-in.

280030-003

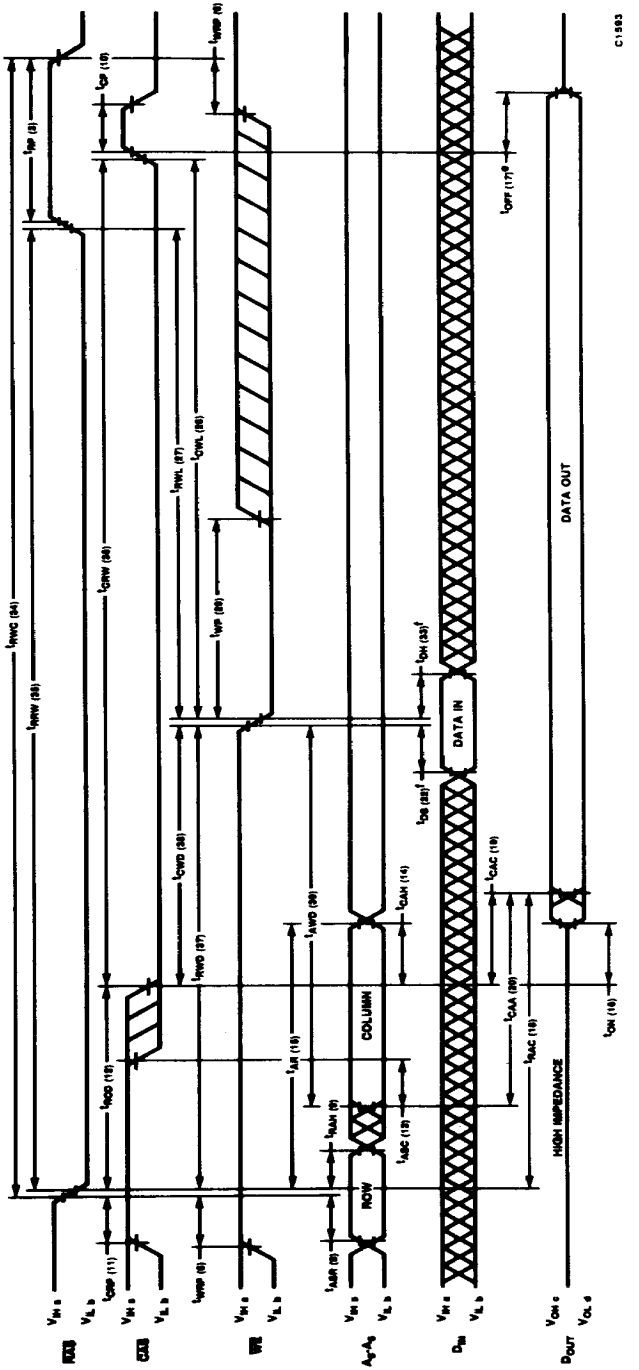
WAVEFORMS (Cont.)
Write Cycle ($\overline{WE}$ Controlled)[f]



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches the data-in.

280030-003

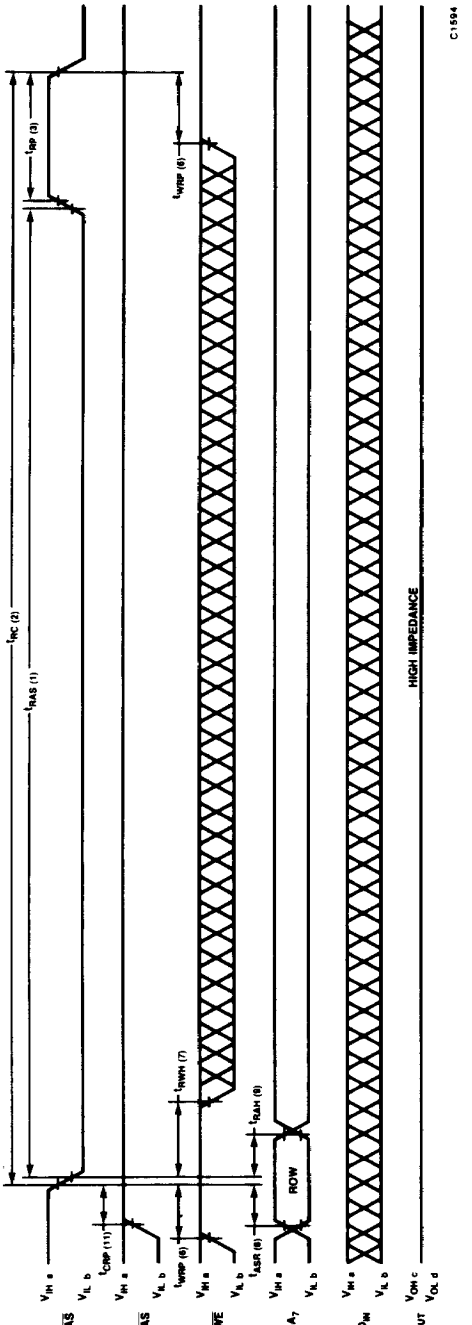
WAVEFORMS (Cont.)
Read/Modify/Write Cycle



NOTES: a.b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
f. t_{OS} and t_{OH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

280030-003

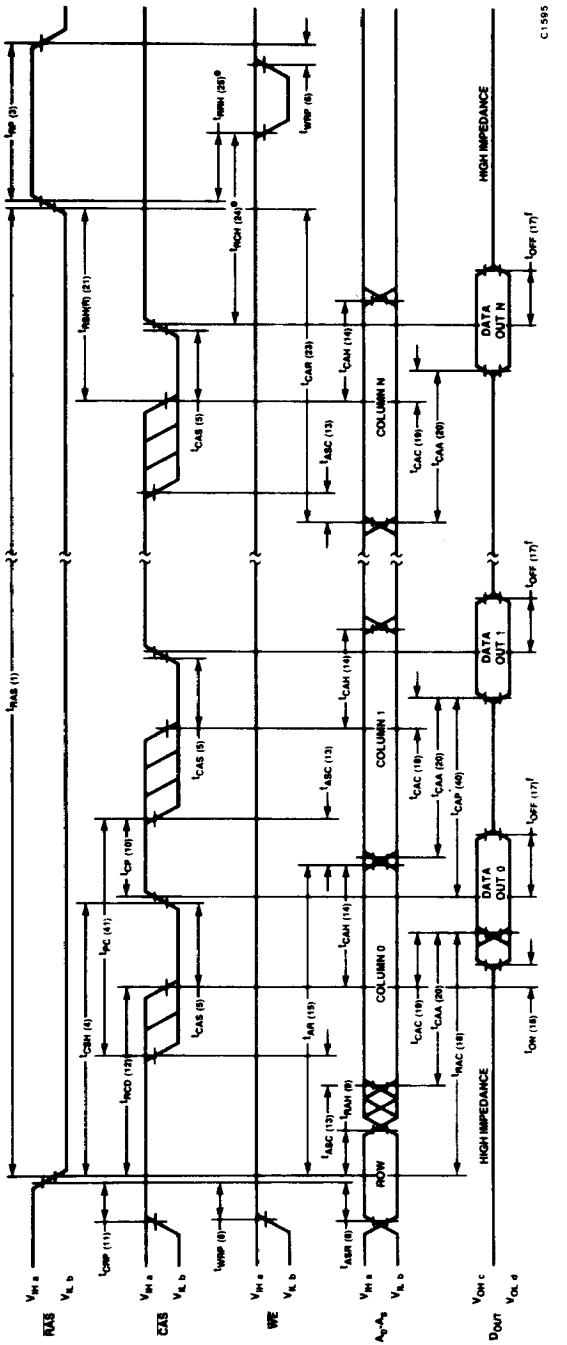
WAVEFORMS (Cont.)
RAS-Only Refresh Cycle



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

280030-003

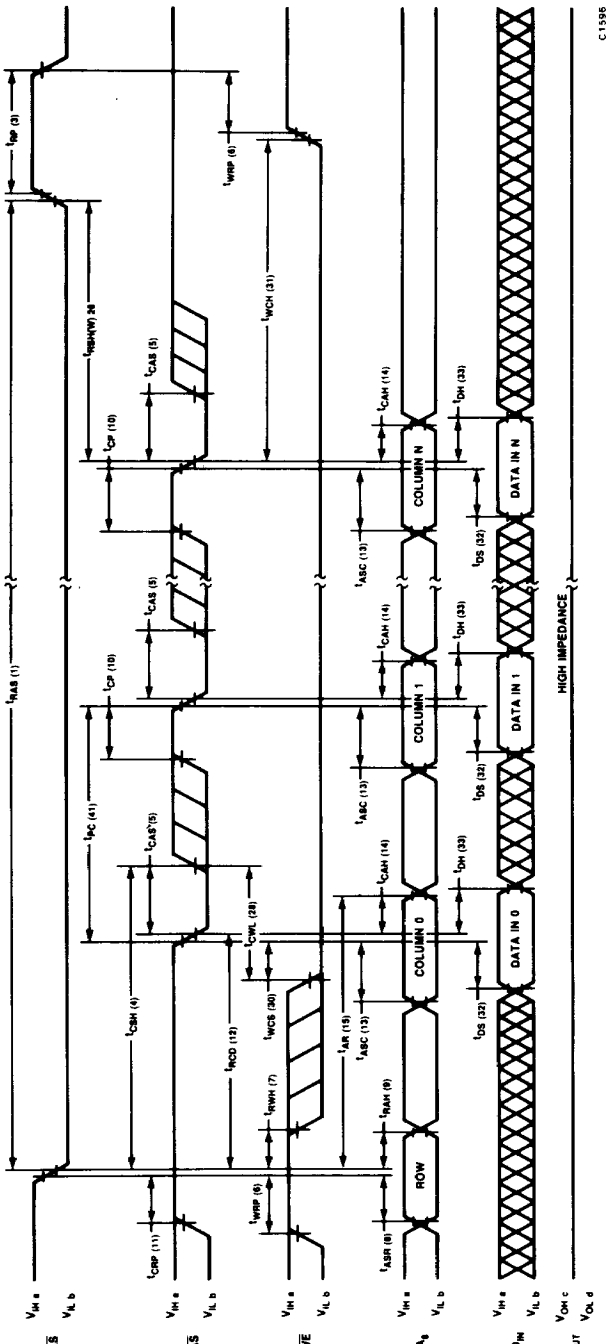
WAVEFORMS (Cont.)
Ripplemode Read Cycle



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}
e. Either t_{RCH} or t_{RRH} must be satisfied.
f. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

280030-003

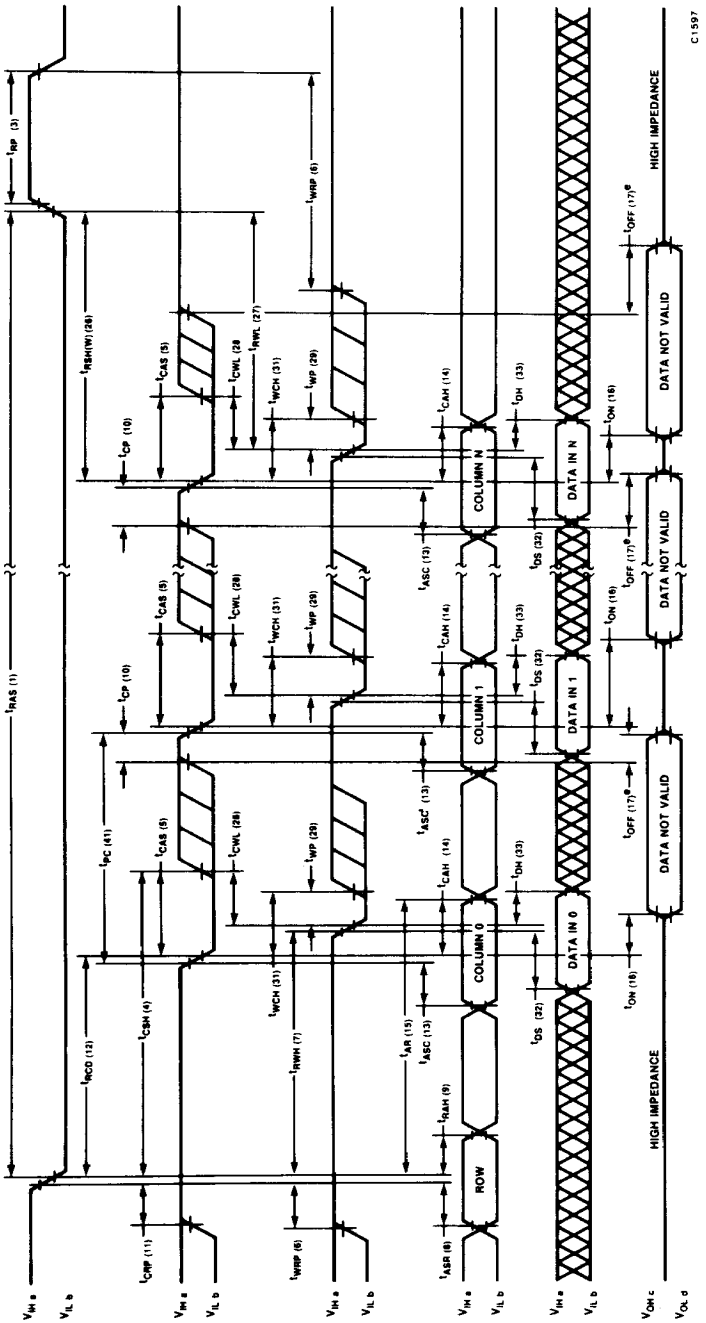
WAVEFORMS (Cont.)
Ripplemode Write Cycle ($\overline{CAS}$ Controlled)[e]



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ latches column addresses and data-in.

280030-003

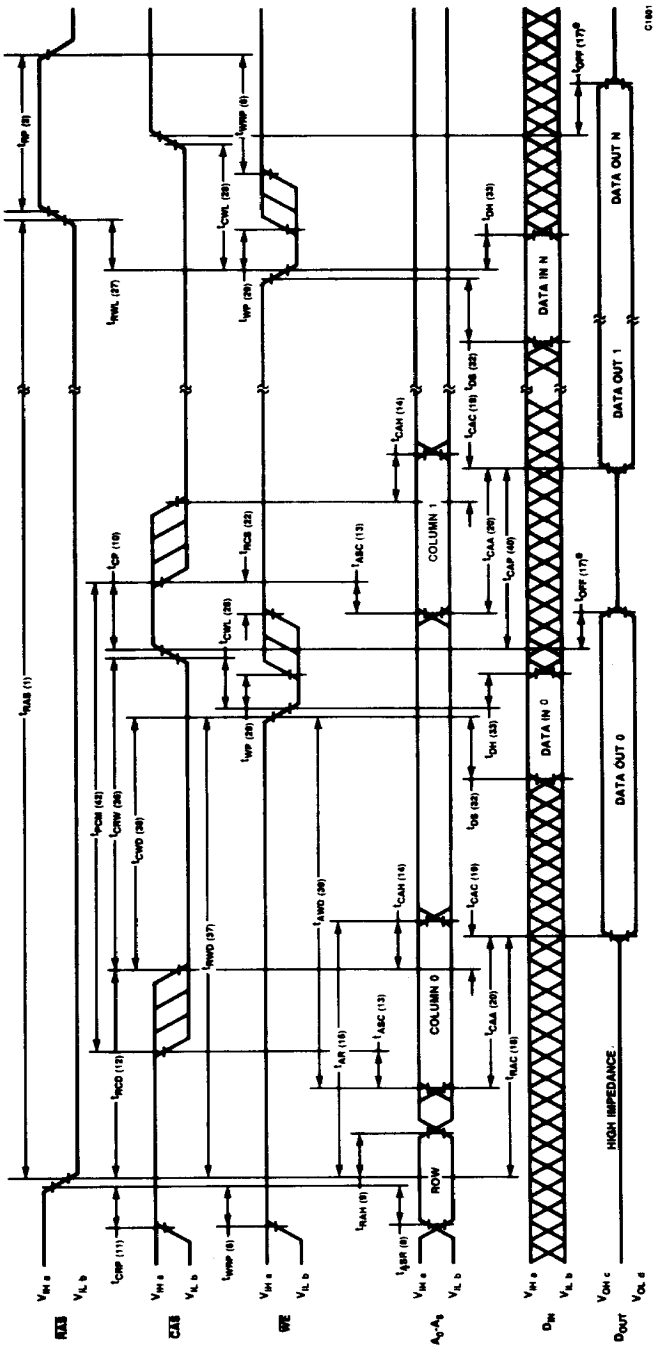
WAVEFORMS (Cont.)
Ripplemode Write Cycle ($\overline{WE}$ Controlled)[f]



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches the data-in.

280030-003

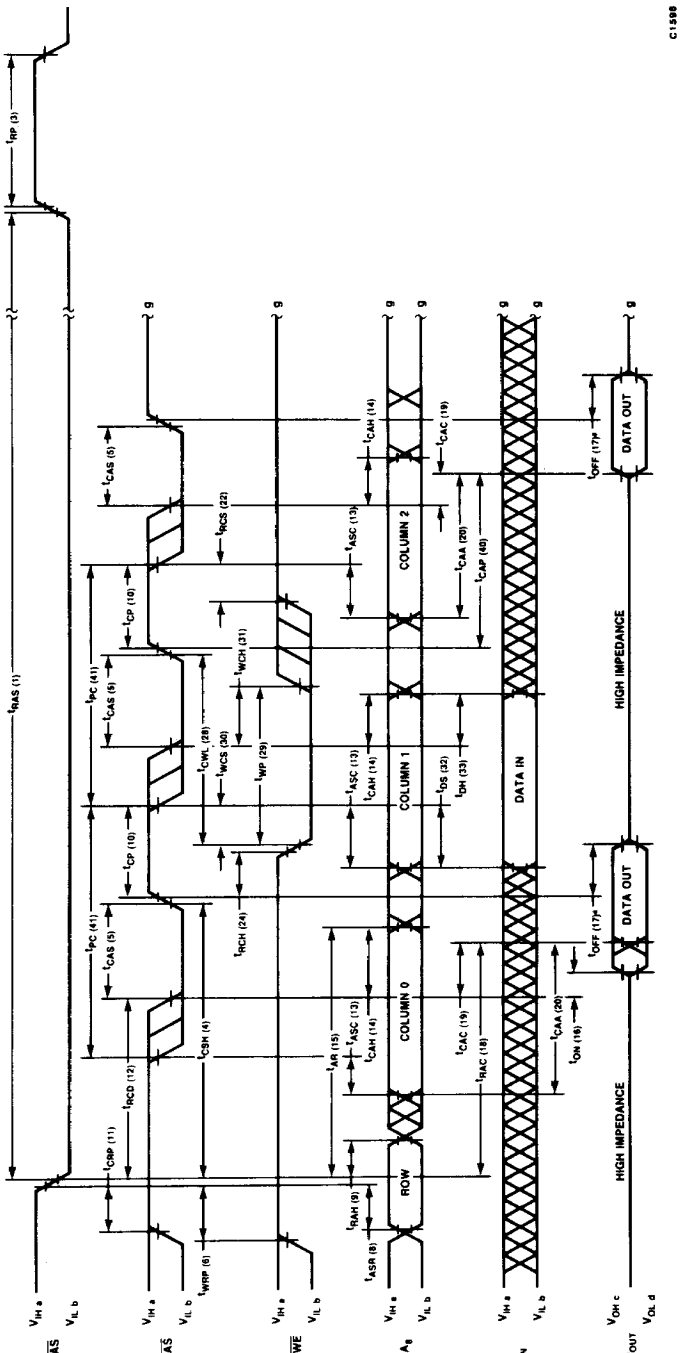
WAVEFORMS (Cont.)
Ripplemode Read/Modify/Write Cycle[f]



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to $\overline{WE}$ low transition. $\overline{CAS}$ latches the column addresses while $\overline{WE}$ latches the data-in.

280030-003

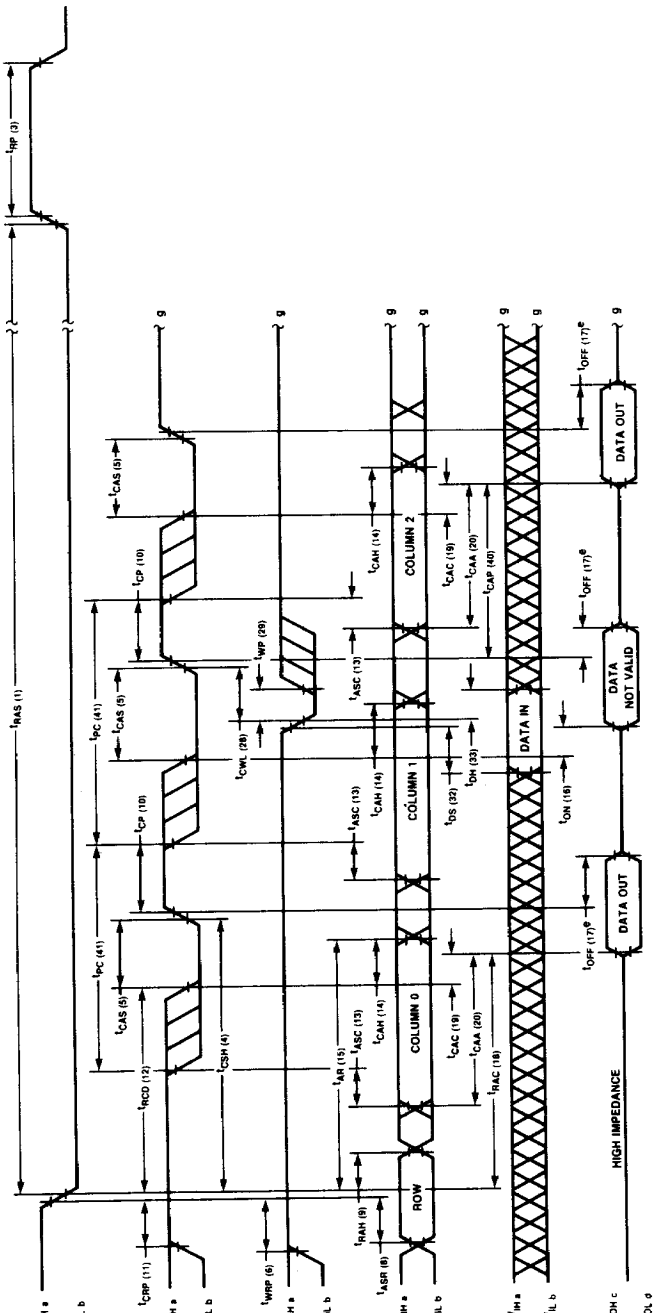
WAVEFORMS (Cont.)
Ripplemode Read/Write/Read/. . . Cycle ($\overline{CAS}$ Controlled)[f]



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
f. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ latches column addresses and data-in.
g. The cycle can be terminated either by a read or a write operation followed by a $\overline{RAS}$ high transition. See page 11 or 12 for timings.

280030-003

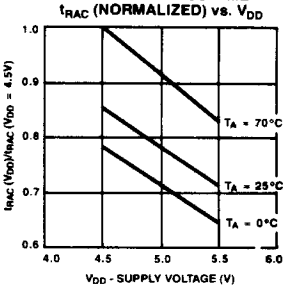
WAVEFORMS (Cont.)
Ripplemode Read/Write/Read/. . . Cycle ($\overline{WE}$ Controlled)[f]



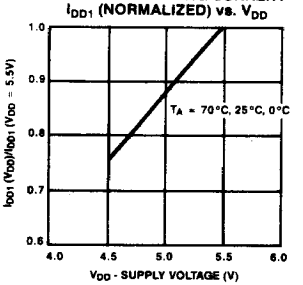
NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to $\overline{WE}$ low transition. $\overline{CAS}$ latches the column addresses while $\overline{WE}$ latches data-in.
g. The cycle can be terminated either by a read or a write operation followed by a $\overline{RAS}$ high transition. See page 11 or 13 for timings.

280030-003

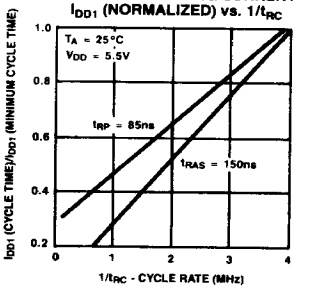
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) vs. V_{DD}



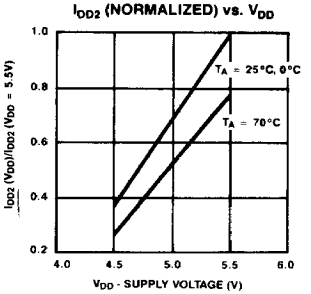
GRAPH 2
TYPICAL OPERATING CURRENT
I_{DD1} (NORMALIZED) vs. V_{DD}



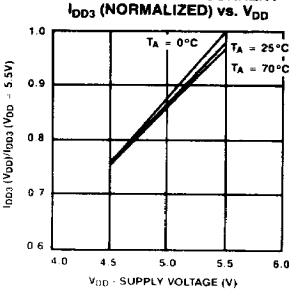
GRAPH 3
TYPICAL OPERATING CURRENT
I_{DD1} (NORMALIZED) vs. $1/t_{RC}$



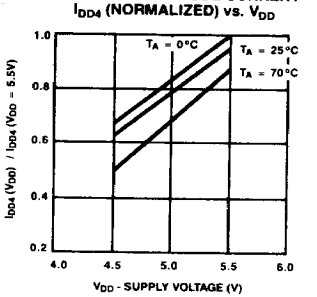
GRAPH 4
TYPICAL TTL STANDBY CURRENT
I_{DD2} (NORMALIZED) vs. V_{DD}



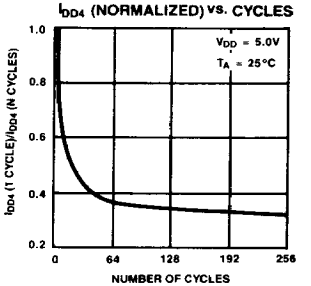
GRAPH 5
TYPICAL REFRESH CURRENT
I_{DD3} (NORMALIZED) vs. V_{DD}



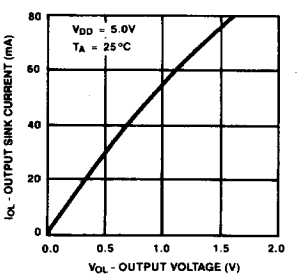
GRAPH 6
TYPICAL RIPPLEMODE CURRENT
I_{DD4} (NORMALIZED) vs. V_{DD}



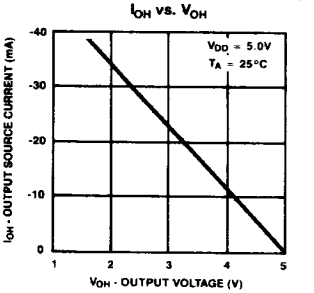
GRAPH 7
TYPICAL RIPPLEMODE CURRENT
I_{DD4} (NORMALIZED) vs. CYCLES



GRAPH 8
TYPICAL OUTPUT SINK CURRENT
I_{OL} vs. V_{OL}



GRAPH 9
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} vs. V_{OH}

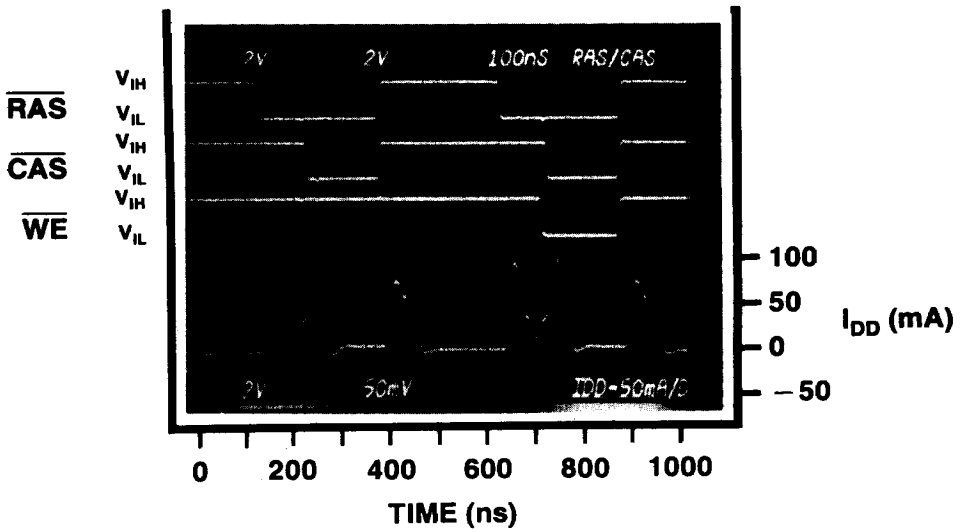


1687

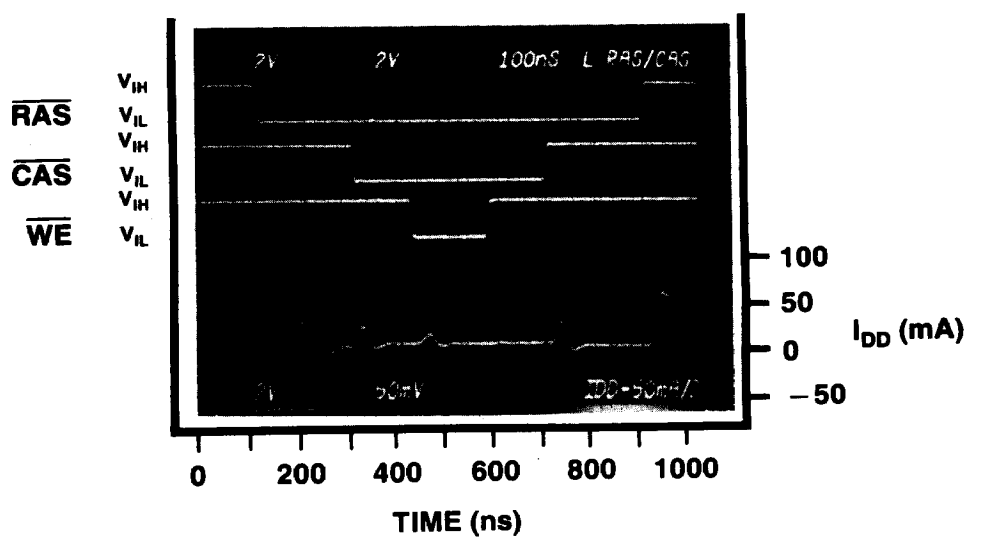
280030-003

Typical power supply waveforms versus time are shown for the $\overline{RAS}/\overline{CAS}$ timings of the Read/Write, $\overline{RAS}$-Only refresh and Ripplemode cycles.

$\overline{RAS}/\overline{CAS}$

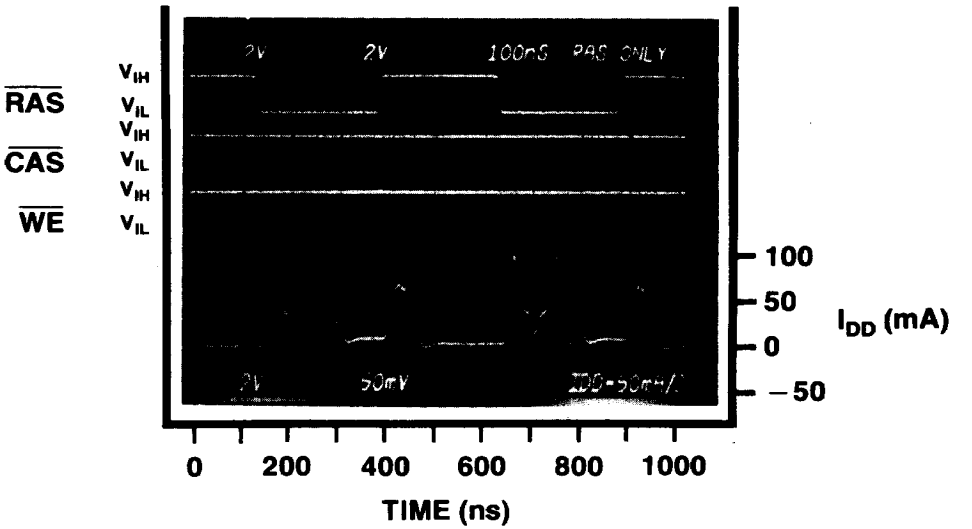


LONG $\overline{RAS}/\overline{CAS}$

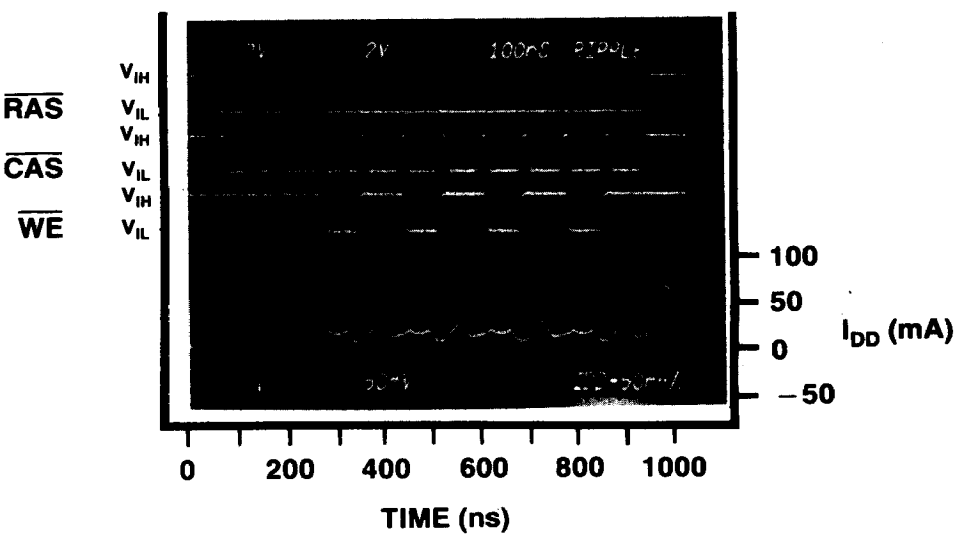


280030-003

$\overline{RAS}$-ONLY REFRESH



RIPPLEMODE™



280030-003

FUNCTIONAL DESCRIPTION

The 51C256H is a CHMOS dynamic RAM optimized for high data bandwidth applications. The functionality is similar to a traditional dynamic RAM. The 51C256H reads and writes data by multiplexing an 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent upon a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

Memory Cycle

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP}, has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out becomes valid only when t_{RAC}, t_{CAA}, and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched in by $\overline{CAS}$. The write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the later of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ will maintain the output in the high impedance state; terminating with $\overline{WE}$ allows the output to go active.

The 51C256H incorporates a self-timed write feature which simplifies the system interface. The write function is internally timed on a write command which allows for a fast write pulse width and a fast write precharge time, thus eliminating the need for critical placement of transitions during the write cycle.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only cycle will perform refresh.

Ripplemode™ Operation

Ripplemode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are performed, retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the addresses into the column address buffer and acts as an output enable.

During this operation read, write, read-modify-write, or read-write-read cycles are possible at random or sequential addresses within a row. Following the entry cycle into Ripplemode operation, access time is t_{CAA} or t_{CAP} dependent. If the column address is valid prior to or coincident with the rising edge of $\overline{CAS}$, then the access time is determined by the rising edge of $\overline{CAS}$ specified by t_{CAP} as shown in Figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{CAA}. For both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Data Out Operation

The 51C256H Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μS is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of the

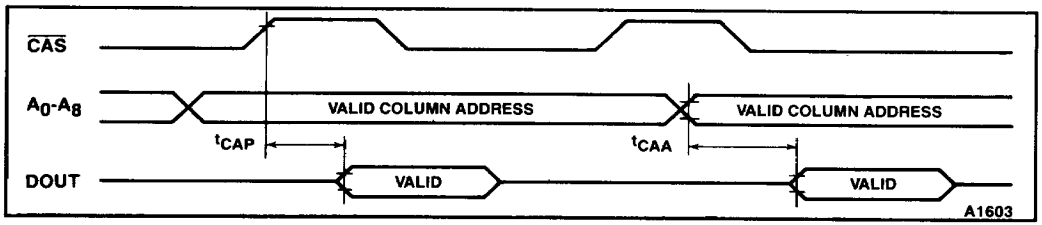


Figure 1. Ripplemode™ Access Time Determination

cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).

The V_{DD} current (I_{DD}) requirement of the 51C256H during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS} = V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

Table 1. Intel 51C256H Data Output Operation for Various Types of Cycles

Cycle	Data Out of State
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Read-Write-Read Cycle ($\overline{CAS}$ Controlled)	Data from Addressed Memory Cell
Read-Write-Read Cycle ($\overline{WE}$ Controlled)	Data from Addressed Memory Cell and Active, Not Valid
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Only Cycle	High Impedance