Section 2. VGA Function

Notes:

VGA Function Introduction

The basic system video is generated by the Type 1 or Type 2 video subsystem. The circuitry that provides the VGA function includes a video buffer, a video digital-to-analog converter (DAC), and test circuitry. Video memory is mapped as four planes of 64Kb by 8 bits (maps 0 through 3). The video DAC drives the analog output to the display connector. The test circuitry determines the type of display attached, color or monochrome.

The video subsystem controls the access to video memory from the system and the cathode-ray tube (CRT) controller. It also controls the system addresses assigned to video memory. Up to three starting addresses can be programmed for compatibility with previous video adapters.

In the graphics modes, the mode determines the way video information is formatted into memory, and the way memory is organized.

In alphanumeric modes, the system writes the ASCII character code and attribute data to video memory maps 0 and 1, respectively. Memory map 2 contains the character font loaded by BIOS during an alphanumeric mode set. The font is used by the character generator to create the character image on the display.

Three fonts are contained in read-only memory (ROM): an 8-by-8 font, an 8-by-14 font, and an 8-by-16 font. Up to eight 256-character fonts can be loaded into the video memory map 2; two of these fonts can be active at one time, allowing a 512-character font.

The video subsystem formats the information in video memory and sends the output to the video DAC. For color displays, the video DAC sends three analog color signals (red, green, and blue) to the display connector. For monochrome displays, BIOS translates the color information in the DAC, and the DAC drives the summed signal onto the green output.

The auxiliary video connector allows video data to be passed between the video subsystem and an adapter plugged into the channel connector.

When it is disabled, the video subsystem will not respond to video memory or I/O reads or writes; however, the video image continues to be displayed.

Note: Compatibility with other hardware is best achieved by using the BIOS interface or operating system interface whenever possible.

The following is a diagram of the VGA function.

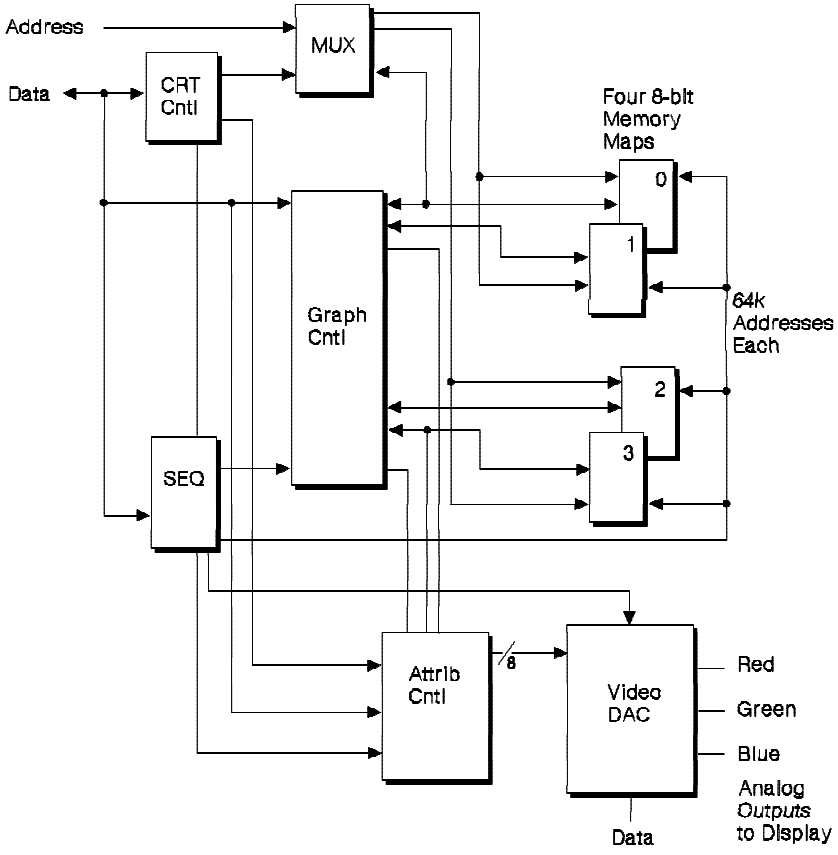


Figure 2-1. Diagram of the VGA Function

Major Components

The video subsystem contains all circuits necessary to generate the timing for the video memory and generates the video information going to the video DAC. The major components are: ROM BIOS, the support logic, and the Video Graphics Array interface.

ROM BIOS

BIOS provides software support and contains the character fonts and the system interface to run the video subsystem.

Support Logic

The support logic consists of the video memory, the clocks, and the video DAC. The video memory consists of at least 256KB; its use and mapping depend on the mode selected.

Two clock sources provide the dot rate. The clock source is selected in the Miscellaneous Output register.

The video DAC contains the color palette that is used to convert the video data into the video signal sent to the display. Three analog signals (red, green, and blue) are output from the DAC.

The maximum number of colors displayed is 256 out of 256K, and the maximum number of gray shades is 64 out of 64.

VGA Components

The VGA function has four major functional areas: the CRT controller, the sequencer, the graphics controller, and the attribute controller.

CRT Controller

The CRT controller generates horizontal and vertical synchronization signal timings, addressing for the regenerative buffer, cursor and underline timings, and refresh addressing for the video memory.

Sequencer

The sequencer generates basic memory timings for the video memory and the character clock for controlling regenerative buffer fetches. It allows the system to access memory during active display intervals by periodically inserting dedicated system microprocessor memory cycles between the display memory cycles. Map mask registers in the sequencer are available to protect entire memory maps from being changed.

Graphics Controller

The graphics controller is the interface between the video memory and the attribute controller during active display times, and between video memory and the system microprocessor during memory accesses.

During active display times, memory data is latched and sent to the attribute controller. In graphics modes, the memory data is converted from parallel to serial bit-plane data before being sent; in alphanumeric modes, the parallel attribute data is sent.

During system accesses of video memory, the graphics controller can perform logical operations on the memory data before it reaches video memory or the system data bus. These logical operations are composed of four logical write modes and two logical read modes. The logical operators allow enhanced operations, such as a color compare in the read mode, individual bit masking during write modes, internal 32-bit writes in a single memory cycle, and writing to the display buffer on nonbyte boundaries.

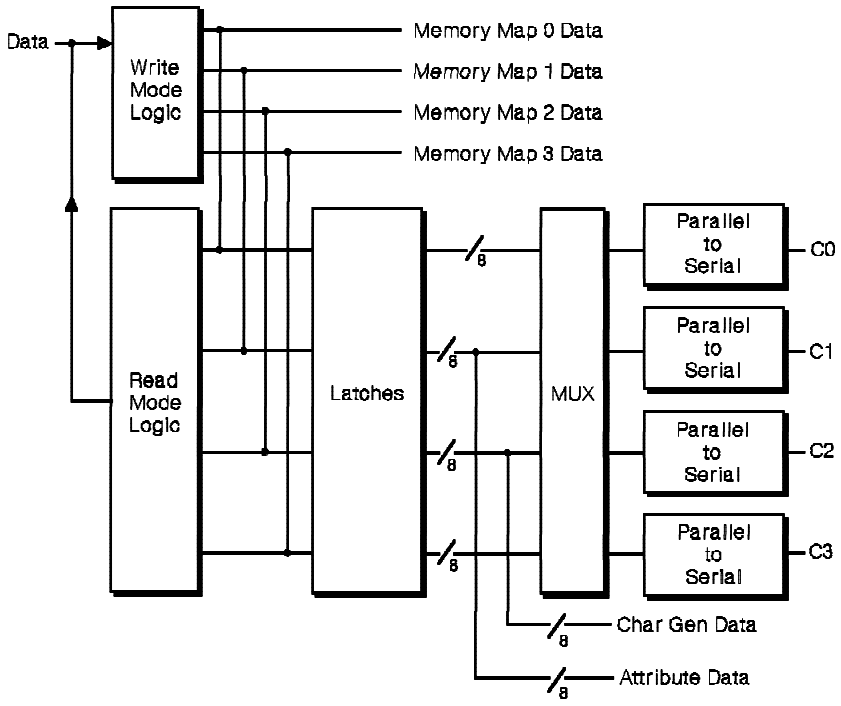


Figure 2-2. Graphics Controller

Attribute Controller

The attribute controller takes in data from video memory through the graphics controller and formats it for display. Attribute data in alphanumeric mode and serialized bit-plane data in graphics mode are converted to an 8-bit color value.

Each color value is selected from an internal color palette of 64 possible colors (except in 256-color mode). The color value is used as a pointer into the video DAC where it is converted to the analog signals that drive the display.

Blinking, underlining, cursor insertion, and PEL panning are also controlled in the attribute controller.

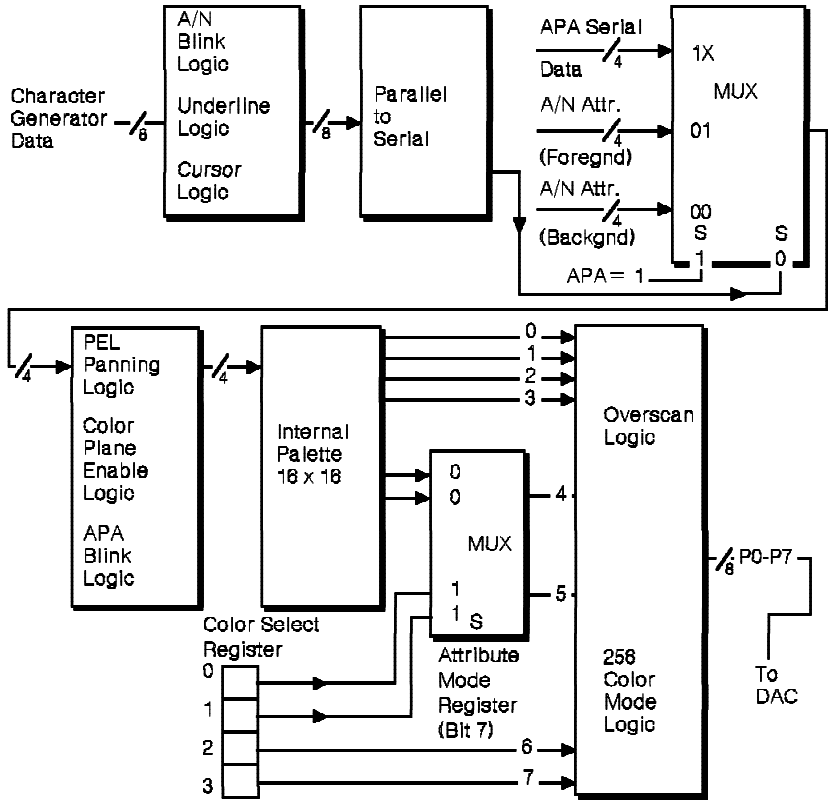


Figure 2-3. Attribute Controller

Hardware Considerations

The following are hardware characteristics of the Type 2 video subsystem that must be considered to ensure program compatibility with the Type 1 video subsystem.

Performance: Type 2 video generally runs faster than the Type 1 video subsystem; programs that depend on execution time of the video subsystem will operate differently.

Video Buffer Compatibility: For each of the video modes, the Type 2 video subsystem maintains a memory mapping that is the same as the Type 1. To maintain this compatibility, the internal addresses to video memory are manipulated so that video memory looks the same. When switching video modes, video data may not be at the same address in video memory.

BIOS calls to set and change modes make allowances for changes in addresses, and should be used for all mode switches.

Character Generator: Differences in the character generator for the Type 2 video subsystem increase the time it takes to load a new font. Because of the additional load time, there is a chance of briefly observing spurious data on the display. BIOS compensates for this during video mode sets.

Register Differences: The following bits for the Type 2 video subsystem differ from the Type 1:

- Bits 2 and 4 in the Clocking Mode register
- Bits 5 and 6 in the End Horizontal Blanking register
- Bits 2 and 4 in the Preset Row Scan register
- Bit 5 in the Address register of the attribute controller.

Modes of Operation

Certain modes on previous IBM display adapters distinguished between monochrome and color displays. For example, mode 0 was the same as mode 1 with the color burst turned off. Because color burst is not supported by the PS/2 video, the mode pairs are exactly the same. The support logic for the VGA function recognizes the type of display, and adjusts the output accordingly. When a monochrome display is attached, the colors for the color modes appear as shades of gray.

Mode 3+ is the default mode with a color display attached and mode 7+ is the default mode with a monochrome display attached.

The following figure describes the alphanumeric (A/N) and all points addressable (APA) graphics modes supported by BIOS. Each color is selected from 256K possibilities, and gray shades from 64 possibilities. The variations within the basic BIOS modes are selected through BIOS calls that set the number of scan lines. The scan line count is set before the mode call is made.

Mode (hex)	Type	Colors	Alpha Format	Buffer Start	Box Size	Max. Pgs.	Freq.	Vert. PELs
0,1	A/N	16	40x25	B8000	8 x 8	8	70Hz	320x200
0*,1*	A/N	16	40x25	B8000	8x14	8	70Hz	320x350
0+,1+	A/N	16	40x25	B8000	9x16	8	70Hz	360x400
2,3	A/N	16	80x25	B8000	8x8	8	70Hz	640x200
2*,3*	A/N	16	80x25	B8000	8x14	8	70Hz	640x350
2+,3+	A/N	16	80x25	B8000	9x16	8	70Hz	720x400
4,5	APA	4	40x25	B8000	8x8	1	70Hz	320x200
6	APA	2	80x25	B8000	8x8	1	70Hz	640x200
7	A/N	–	80x25	B0000	9x14	8	70Hz	720x350
7+	A/N	–	80x25	B0000	9x16	8	70Hz	720x400
D	APA	16	40x25	A0000	8x8	8	70Hz	320x200
E	APA	16	80x25	A0000	8x8	4	70Hz	640x200
F	APA	–	80x25	A0000	8x14	2	70Hz	640x350
10	APA	16	80x25	A0000	8x14	2	70Hz	640x350
11	APA	2	80x30	A0000	8x16	1	60Hz	640x480
12	APA	16	80x30	A0000	8x16	1	60Hz	640x480
13	APA	256	40x25	A0000	8x8	1	70Hz	320x200

Note: * or + Enhanced modes

Figure 2-4. BIOS Video Modes

In the 200-scan-line modes, the data for each scan line is scanned twice. This double scanning allows the 200-scan-line image to be displayed in 400 scan lines.

Border support and double scanning depend on the mode selected. The following shows which modes use double scanning and which support a border.

Mode (Hex)	Double Scan	Border Support
0, 1	Yes	No
0*, 1*	No	No
0+, 1+	No	No
2, 3	Yes	Yes
2*, 3*	No	Yes
2+, 3+	No	Yes
4, 5	Yes	No
6	Yes	Yes
7	No	Yes
7+	No	Yes
D	Yes	No
E	Yes	Yes
F	No	Yes
10	No	Yes
11	No	Yes
12	No	Yes
13	Yes	Yes

Note: * or + Enhanced modes

Figure 2-5. Double Scanning and Border Support

Display Support

The video subsystem supports direct-drive analog displays. The displays must have a horizontal scan rate of 31.5 kHz, and a vertical scan rate capability of 50 to 70 Hz. Displays that use a digital input, such as the IBM Color Display, are *not* supported. The following figure summarizes the minimum display characteristics required to support VGA mode operation.

Parameter	Color	Monochrome
Horizontal Scan Rate	31.5 kHz	31.5 kHz
Vertical Scan Rate	50 to 70 Hz	50 to 70 Hz
Video Bandwidth	28 MHz	28 MHz
Maximum Horizontal Resolution	720 PELs	720 PELs
Maximum Vertical Resolution	480 Lines	480 Lines

Figure 2-6. Direct-Drive Analog Displays

Since color and monochrome displays run at the same scan rate, all modes work on both displays. The vertical gain of the display is controlled by the polarity of the vertical and horizontal synchronization pulses. This is done so 350, 400, or 480 lines can be displayed without adjusting the display. See “Signal Timing” on page 4-3 for more information.

Programmable Option Select

The video subsystem supports programmable option select (POS). The video subsystem is placed in the setup mode through the System Board Setup/Enable register (hex 0094). (For more information, see the system-specific sections.) For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Alphanumeric Modes

The alphanumeric modes are modes hex 0 through 3 and 7. The mode chart lists the variations of these modes (see Figure 2-4 on page 2-12). The data format for alphanumeric modes is the same as the data format on the IBM Color/Graphics Monitor Adapter, the IBM Monochrome Display Adapter, and the IBM Enhanced Graphics Adapter.

BIOS initializes the video subsystem according to the selected mode and loads the color values into the video DAC. These color values can be changed to give a different color set to select from. Bit 3 of the attribute byte can be redefined by the Character Map Select register to act as a switch between character sets, giving the programmer access to 512 characters at one time.

When an alphanumeric mode is selected, the BIOS transfers character font patterns from the ROM to map 2. The system stores the character data in map 0, and the attribute data in map 1. In the alphanumeric modes, the programmer views maps 0 and 1 as a single buffer. The CRT controller generates sequential addresses and fetches one character code byte and one attribute byte at a time. The character code and row scan count are combined to make up the address into map 2, which contains the character font. The appropriate dot patterns are then sent to the attribute controller, where color is assigned according to the attribute data.

Every display-character position in the alphanumeric mode is defined by two bytes in the display buffer. Both the color/graphics and the monochrome emulation modes use the following 2-byte character/attribute format.

.

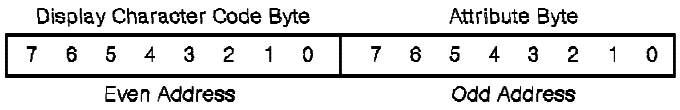


Figure 2-7. Character/Attribute Format

See “Characters and Keystrokes” for characters loaded during a BIOS mode set.

The functions of the attribute bytes are defined in the following table. Bit 7 can be redefined in the Attribute Mode Control register to give 16 possible background colors; its default is to control character blinking. Bit 3 can be redefined in the Character Map Select register to select between two character fonts; its default is to control foreground color selection.

Bit	Color	Function
7	B/I	Blinking or Background Intensity
6	R	Background Color
5	G	Background Color
4	B	Background Color
3	I/CS	Foreground Intensity or Character Font Select
2	R	Foreground Color
1	G	Foreground Color
0	B	Foreground Color

Figure 2-8. Attribute Byte Definitions

For more information about the attribute bytes, see “Character Map Select Register” on page 2-52 and “Attribute Mode Control Register” on page 2-92.

The following are the color values loaded by BIOS for the 16-color modes.

Intensity	Red	Green	Blue	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	White
1	0	0	0	Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White (High Intensity)

Figure 2-9. BIOS Color Set

Both 40-column and 80-column alphanumeric modes are supported. The features of the 40-column alphanumeric modes (all variations of modes hex 0 and 1) are:

- 25 rows of 40 characters
- 2000 bytes of video memory per page
- One character byte and one attribute byte per character.

The features of the 80-column alphanumeric modes (all variations of modes hex 2, 3, and 7) are:

- 25 rows of 80 characters
- 4000 bytes of video memory per page
- One character byte and one attribute byte per character.

Graphics Modes

The graphics modes supported in BIOS are modes hex 4, 5, 6, F, and 11. The colors described in this section are generated when the BIOS is used to set the mode. BIOS initializes the video subsystem and the DAC palette to generate these colors. If the DAC palette is changed, different colors are generated.

320 x 200 Four-Color Graphics (Modes Hex 4 and 5)

Addressing, mapping, and data format are the same as the 320 x 200 PEL mode of the IBM Color/Graphics Monitor Adapter. The display buffer is configured at hex B8000. Bit image data is stored in memory maps 0 and 1. The two bit planes (C0 and C1) are each formed from bits from both memory maps.

Features of this mode are:

- A maximum of 200 rows of 320 PELs
- Double scanned to display as 400 rows
- Memory-mapped graphics
- Four colors for each PEL
- Four PELs per byte
- 16,000 bytes of read/write memory.

The video memory is organized into two banks of 8,000 bytes each, using the following format. Address hex B8000 contains the PEL information for the upper-left corner of the display area.

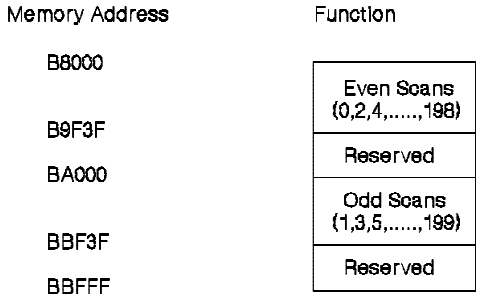


Figure 2-10. Video Memory Format

The following figure shows the format for each byte.

Bit	Function
7	C1 - First Display PEL
6	C0 - First Display PEL
5	C1 - Second Display PEL
4	C0 - Second Display PEL
3	C1 - Third Display PEL
2	C0 - Third Display PEL
1	C1 - Fourth Display PEL
0	C0 - Fourth Display PEL

Figure 2-11. PEL Format, Modes Hex 4 and 5

The color selected depends on the color set that is used. Color set 1 is the default. For information on changing the color set, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Bits C1 C0	Color Selected	
	Color Set 1	**Color Set 0**
0 0	Black	Black
0 1	Light Cyan	Green
1 0	Light Magenta	Red
1 1	Intensified White	Brown

Figure 2-12. Color Selections, Modes Hex 4 and 5

640 x 200 Two-Color Graphics (Mode Hex 6)

Addressing, scan-line mapping, and data format are the same as the 640 x 200 PEL black and white mode of the IBM Color/Graphics Monitor Adapter. The display buffer is configured at hex B8000. Bit image data is stored in memory map 0 and comprises a single bit plane (C0). Features of this mode are:

- A maximum of 200 rows of 640 PELs
- Double scanned to display as 400 rows
- Same addressing and scan-line mapping as 320 x 200 graphics
- Two colors for each PEL
- Eight PELs per byte
- 16,000 bytes of read/write memory.

The following shows the format for each byte.

Bit	Function
7	First Display PEL
6	Second Display PEL
5	Third Display PEL
4	Fourth Display PEL
3	Fifth Display PEL
2	Sixth Display PEL
1	Seventh Display PEL
0	Eighth Display PEL

Figure 2-13. PEL Format, Mode Hex 6

The bit definition for each PEL is 0 equals black and 1 equals intensified white.

640 x 350 Graphics (Mode Hex F)

This mode emulates the EGA graphics with the monochrome display and the following attributes: black, video, blinking video, and intensified video. A resolution of 640 x 350 uses 56,000 bytes of video memory to support the four attributes. This mode uses maps 0 and 2; map 0 is the video bit plane (C0), and map 2 is the intensity bit plane (C2). Both planes reside at address hex A0000.

The two bits, one from each bit plane, define one PEL. The bit definitions are given in the following table.

C2	C0	PEL Color
0	0	Black
0	1	White
1	0	Blinking White
1	1	Intensified White

Figure 2-14. Bit Definitions C2,C0

Memory is organized with successive bytes defining successive PELs. The first eight PELs displayed are defined by the byte at hex A0000, the second eight PELs by the byte at hex A0001, and so on. The most-significant bit in each byte defines the first PEL for that byte.

Since both bit planes reside at address hex A0000, the user must select the plane to update through the Map Mask register of the sequence controller (see “Video Memory Organization” on page 2-24).

640 x 480 Two-Color Graphics (Mode Hex 11)

This mode provides two-color graphics with the same data format as mode 6. Addressing and mapping are shown under “Video Memory Organization” on page 2-24.

The bit image data is stored in map 0 and comprises a single bit plane (C0). The video buffer starts at hex A0000. The first byte contains the first eight PELs; the second byte, at hex A0001, contains the second eight PELs, and so on. The bit definition for each PEL is 0 equals black and 1 equals intensified white.

16-Color Graphics Modes (Modes Hex D, E, 10, and 12)

These modes support 16 colors. For all modes, the bit image data is stored in all four memory maps. Each memory map contains the data for one bit plane. The bit planes are C0 through C3 and represent the following colors:

C0 = Blue
C1 = Green
C2 = Red
C3 = Intensified

The four bits define each PEL on the screen by acting as an address (pointer) into the internal palette in the Extended Graphics mode.

The display buffer resides at address hex A0000. The Map Mask register selects any or all of the maps to be updated when the system writes to the display buffer.

256-Color Graphics Mode (Mode Hex 13)

This mode provides graphics with the capability of displaying 256 colors at one time.

The display buffer is sequential, starts at address hex A0000, and is 64,000 bytes long. The first byte contains the color information for the upper-left PEL. The second byte contains the second PEL, and so on, for 64,000 PELs (320 x 200). The bit image data is stored in all four memory maps and comprises four bit planes. The four bit planes are sampled twice to produce eight bit-plane values that address the video DAC.

In this mode, the internal palette of the video subsystem is loaded by BIOS and should not be changed. The first 16 locations in the external palette, which is in the video DAC, contain the colors compatible with the alphanumeric modes. The second 16 locations contain 16 evenly spaced gray shades. The next 216 locations contain values based on a hue-saturation-intensity model tuned to provide a usable, generic color set that covers a wide range of color values.

The following figure shows the color information that is compatible with the colors in other modes.

PEL Bits 7 6 5 4 3 2 1 0	Color Output
0 0 0 0 0 0 0 0	Black
0 0 0 0 0 0 0 1	Blue
0 0 0 0 0 0 1 0	Green
0 0 0 0 0 0 1 1	Cyan
0 0 0 0 0 1 0 0	Red
0 0 0 0 0 1 0 1	Magenta
0 0 0 0 0 1 1 0	Brown
0 0 0 0 0 1 1 1	White
0 0 0 0 1 0 0 0	Dark Gray
0 0 0 0 1 0 0 1	Light Blue
0 0 0 0 1 0 1 0	Light Green
0 0 0 0 1 0 1 1	Light Cyan
0 0 0 0 1 1 0 0	Light Red
0 0 0 0 1 1 0 1	Light Magenta
0 0 0 0 1 1 1 0	Yellow
0 0 0 0 1 1 1 1	Intensified White

Figure 2-15. Compatible Color Coding

Each color in the palette can be programmed to one of 256K different colors.

The features of this mode are:

- A maximum of 200 rows with 320 PELs
- Double scanned to display as 400 rows
- Memory-mapped graphics
- 256 of 256K colors for each PEL
- One byte per PEL
- 64,000 bytes of video memory.

Video Memory Organization

The display buffer consists of 256KB of dynamic read/write memory configured as four 64KB memory maps.

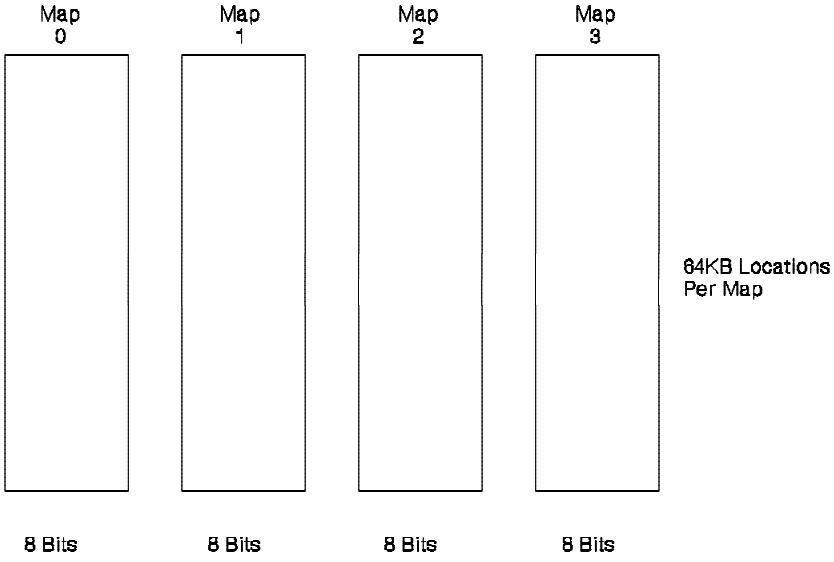


Figure 2-16. 256KB Video Memory Map

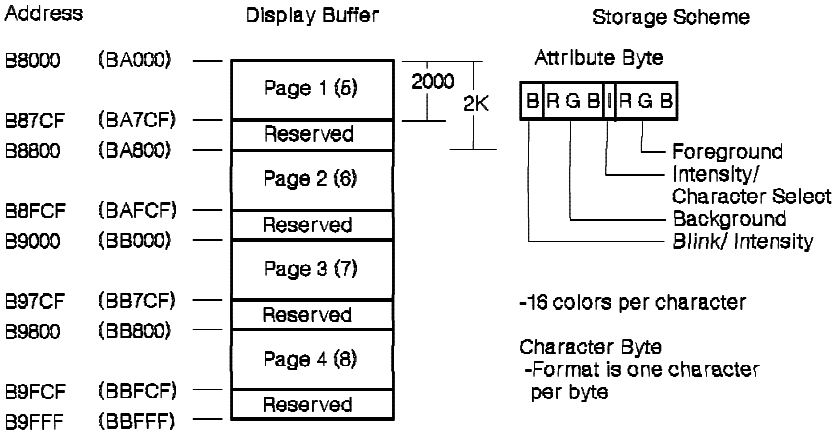
The starting address and size of the display buffer can be changed to maintain compatibility with other display adapters and application software. There are three configurations used by other adapters:

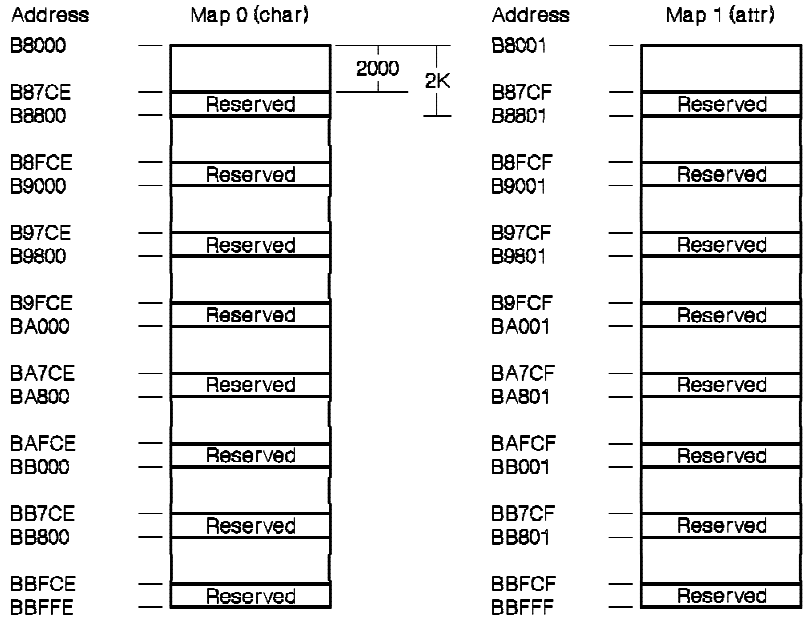
Address hex A0000 for a length of 64KB
Address hex B0000 for a length of 32KB
Address hex B8000 for a length of 32KB.

Memory Modes

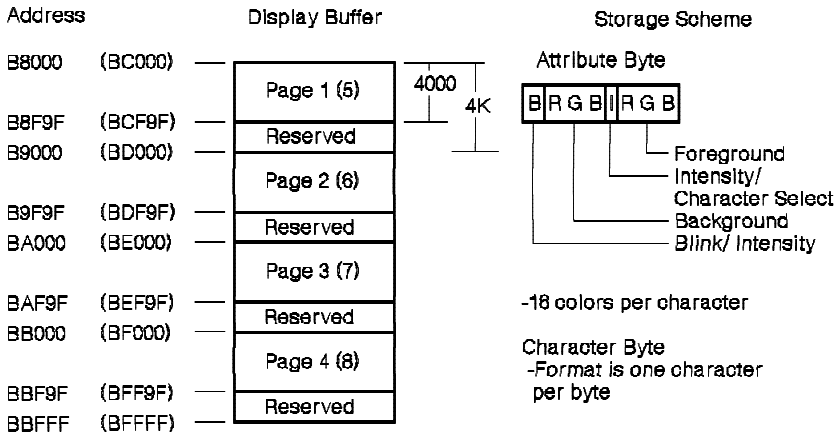
The following pages show the memory organization for each of the BIOS modes.

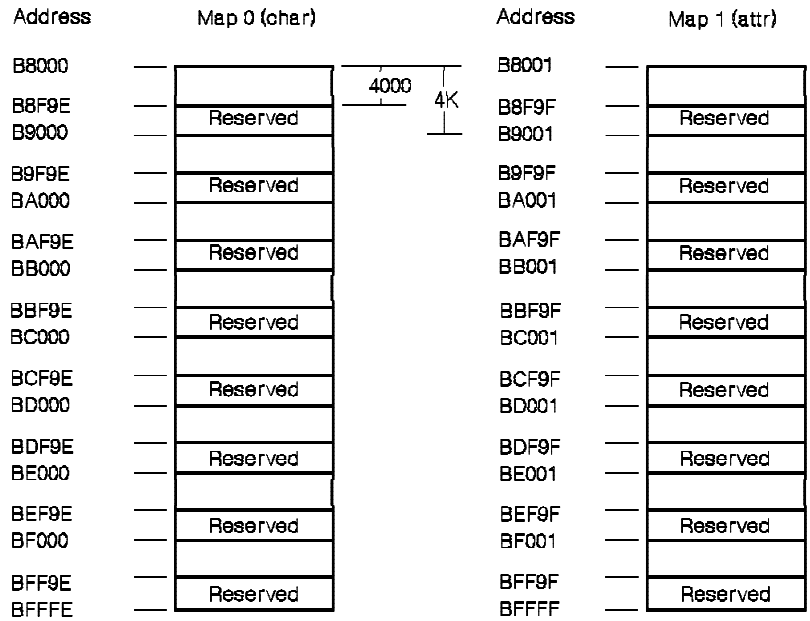
Modes Hex 0, 1


Address
Display Buffer
Storage Scheme
B8000 (BA000)
Page 1 (5)
2000
2K
B87CF (BA7CF)
Reserved
B8800 (BA800)
Page 2 (6)
B8FCF (BAFCF)
Reserved
B9000 (BB000)
Page 3 (7)
B97CF (BB7CF)
Reserved
B9800 (BB800)
Page 4 (8)
B9FCF (BBFCF)
Reserved
B9FFF (BBFFF)
Attribute Byte
B R G B I R G B
Foreground
Intensity/
Character Select
Background
Blink/ Intensity
-16 colors per character
Character Byte
-Format is one character
per byte

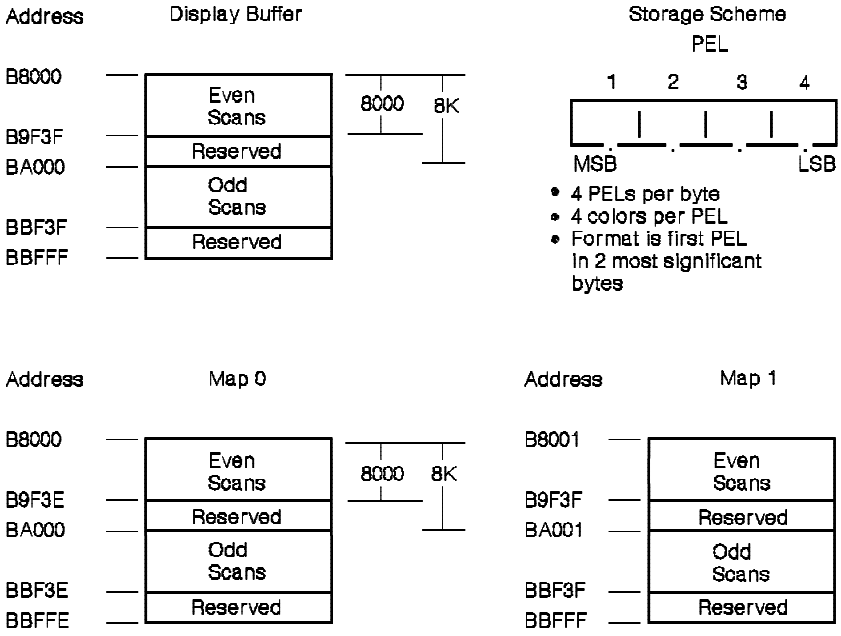

Address
Map 0 (char)
B8000
2000
2K
B87CE
Reserved
B8800
B8FCE
Reserved
B9000
B97CE
Reserved
B9800
B9FCE
Reserved
BA000
BA7CE
Reserved
BA800
BAFCE
Reserved
BB000
BB7CE
Reserved
BB800
BBFCE
Reserved
BBFFE
Address
Map 1 (attr)
B8001
B87CF
Reserved
B8801
B8FCF
Reserved
B9001
B97CF
Reserved
B9801
B9FCF
Reserved
BA001
BA7CF
Reserved
BA801
BAFCF
Reserved
BB001
BB7CF
Reserved
BB801
BBFCF
Reserved
BBFFF

Modes Hex 2, 3

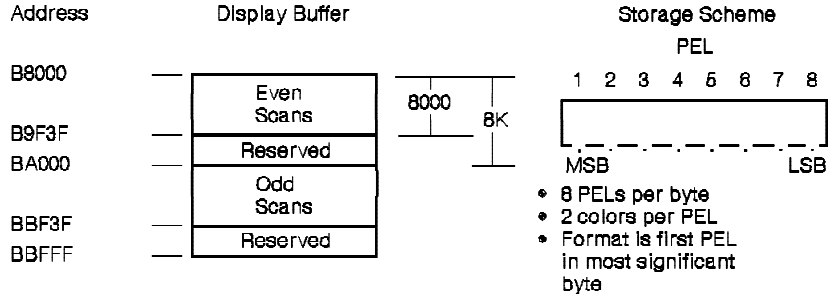

Address
Display Buffer
Storage Scheme
B8000 (BC000)
B8F9F (BCF9F)
B9000 (BD000)
B9F9F (BDF9F)
BA000 (BE000)
BAF9F (BEF9F)
BB000 (BF000)
BBF9F (BFF9F)
BBFFF (BFFFF)
Page 1 (5)
Reserved
Page 2 (6)
Reserved
Page 3 (7)
Reserved
Page 4 (8)
Reserved
4000
4K
Attribute Byte
B R G B I R G B
Foreground
Intensity/
Character Select
Background
Blink/ Intensity
-16 colors per character
Character Byte
-Format is one character
per byte

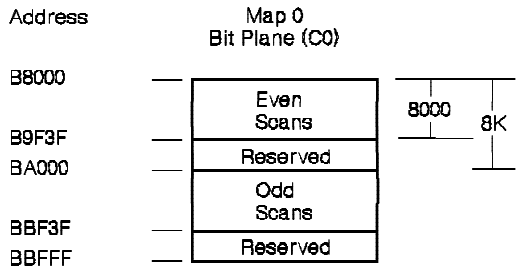

Address
Map 0 (char)
Address
Map 1 (attr)
B8000
B8F9E
B9000
B9F9E
BA000
BAF9E
BB000
BBF9E
BC000
BCF9E
BD000
BDF9E
BE000
BEF9E
BF000
BFF9E
BFFFE
B8001
B8F9F
B9001
B9F9F
BA001
BAF9F
BB001
BBF9F
BC001
BCF9F
BD001
BDF9F
BE001
BEF9F
BF001
BFF9F
BFFFF
Reserved
4000
4K

Modes Hex 4, 5

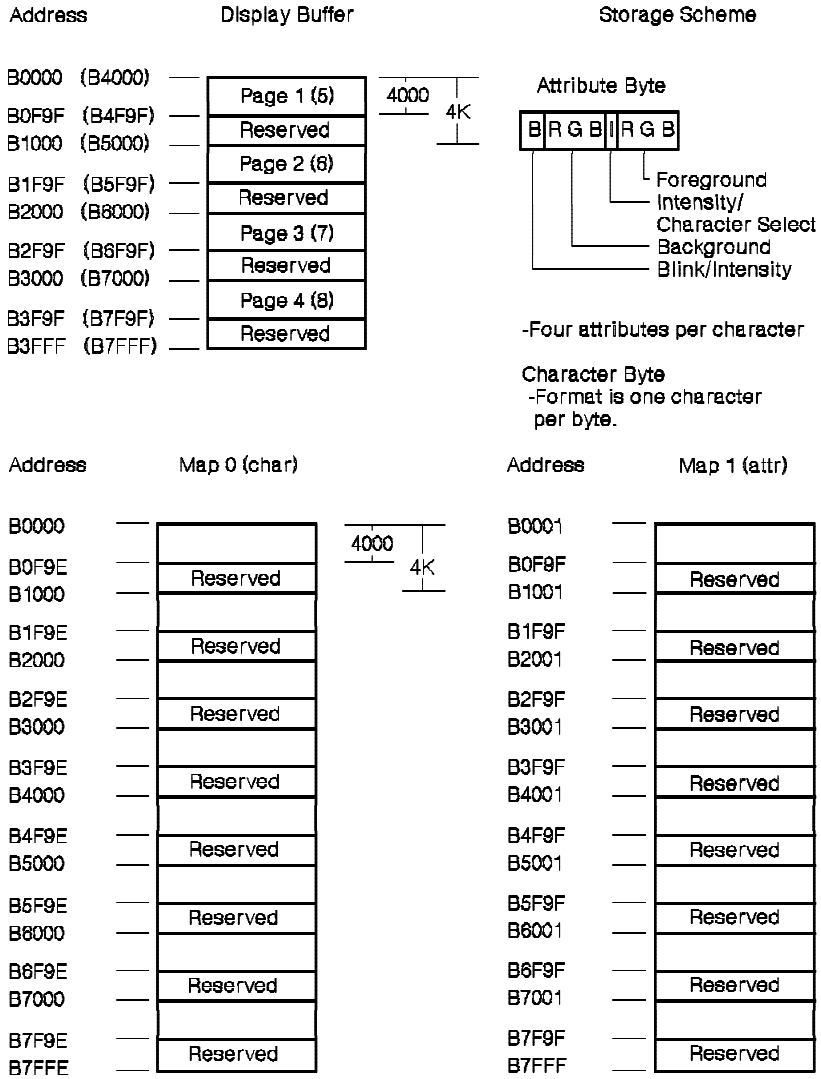

Address
Display Buffer
B8000
B9F3F
BA000
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved
8000
8K
Storage Scheme
PEL
1 2 3 4
MSB
LSB
• 4 PELs per byte
• 4 colors per PEL
• Format is first PEL In 2 most significant bytes
Address
Map 0
B8000
B9F3E
BA000
BBF3E
BBFFE
Even Scans
Reserved
Odd Scans
Reserved
8000
8K
Address
Map 1
B8001
B9F3F
BA001
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved

Mode Hex 6

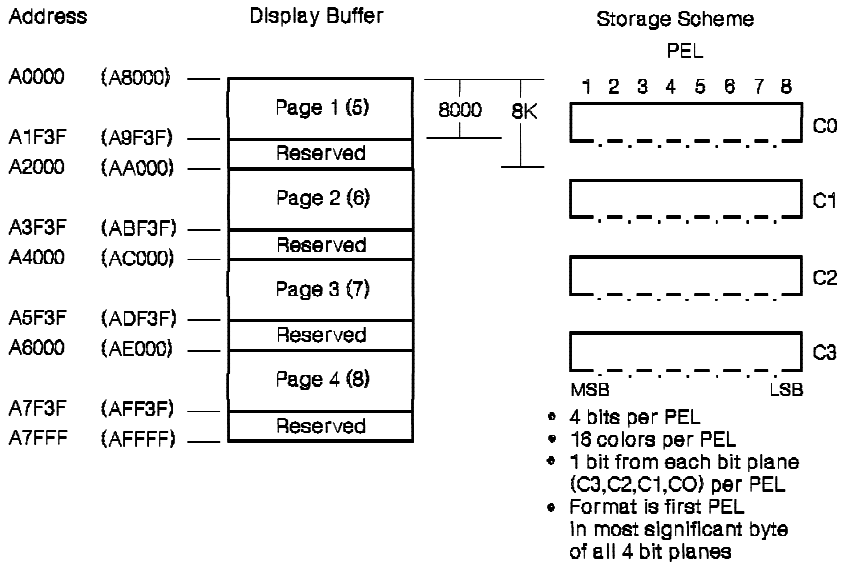

Address
Display Buffer
Storage Scheme
PEL
B8000
B9F3F
BA000
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved
8000
8K
1 2 3 4 5 6 7 8
MSB
LSB
• 8 PELs per byte
• 2 colors per PEL
• Format is first PEL in most significant byte

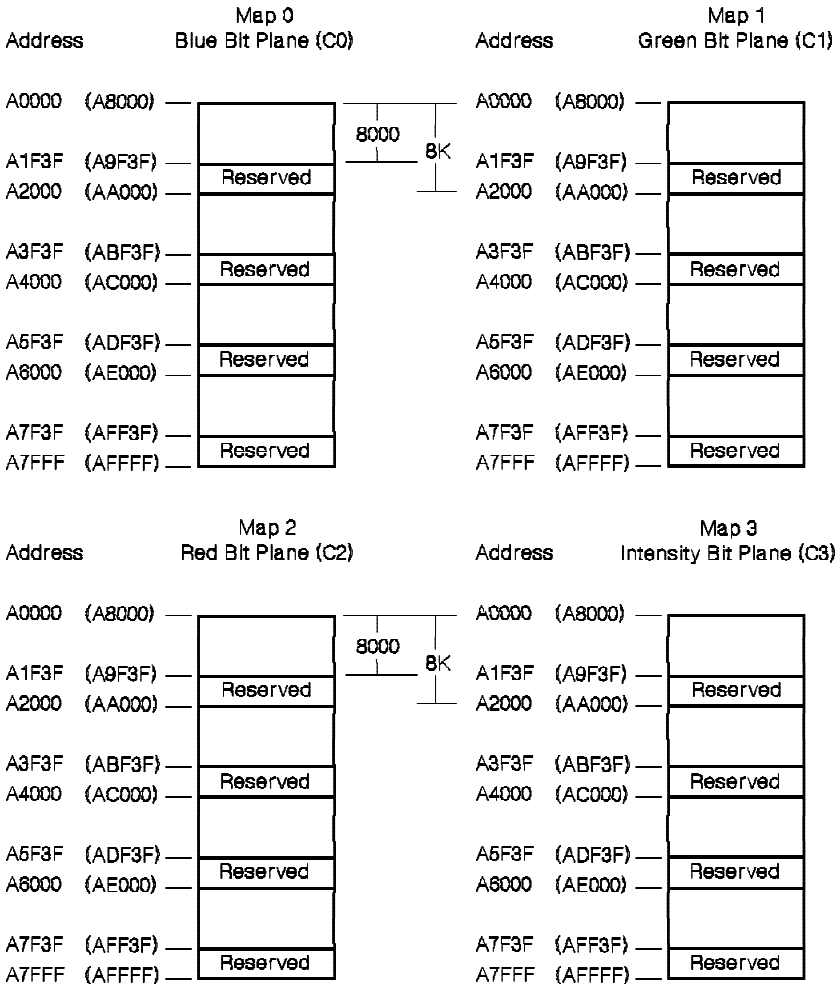

Address
Map 0
Bit Plane (C0)
B8000
B9F3F
BA000
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved
8000
8K

Mode Hex 7

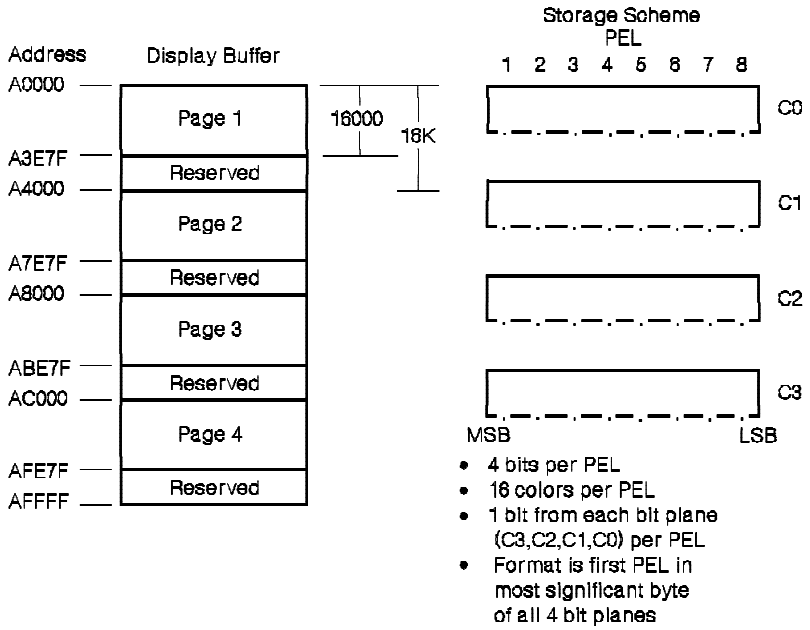

Address
Display Buffer
Storage Scheme
B0000 (B4000)
B0F9F (B4F9F)
B1000 (B5000)
B1F9F (B5F9F)
B2000 (B6000)
B2F9F (B6F9F)
B3000 (B7000)
B3F9F (B7F9F)
B3FFF (B7FFF)
Page 1 (5)
Reserved
Page 2 (6)
Reserved
Page 3 (7)
Reserved
Page 4 (8)
Reserved
4000
4K
Attribute Byte
B R G B I R G B
Foreground Intensity/ Character Select
Background
Blink/Intensity
-Four attributes per character
Character Byte
-Format is one character per byte.
Address
Map 0 (char)
Address
Map 1 (attr)
B0000
B0F9E
B1000
B1F9E
B2000
B2F9E
B3000
B3F9E
B4000
B4F9E
B5000
B5F9E
B6000
B6F9E
B7000
B7F9E
B7FFE
B0001
B0F9F
B1001
B1F9F
B2001
B2F9F
B3001
B3F9F
B4001
B4F9F
B5001
B5F9F
B6001
B6F9F
B7001
B7F9F
B7FFF
Reserved
4000
4K

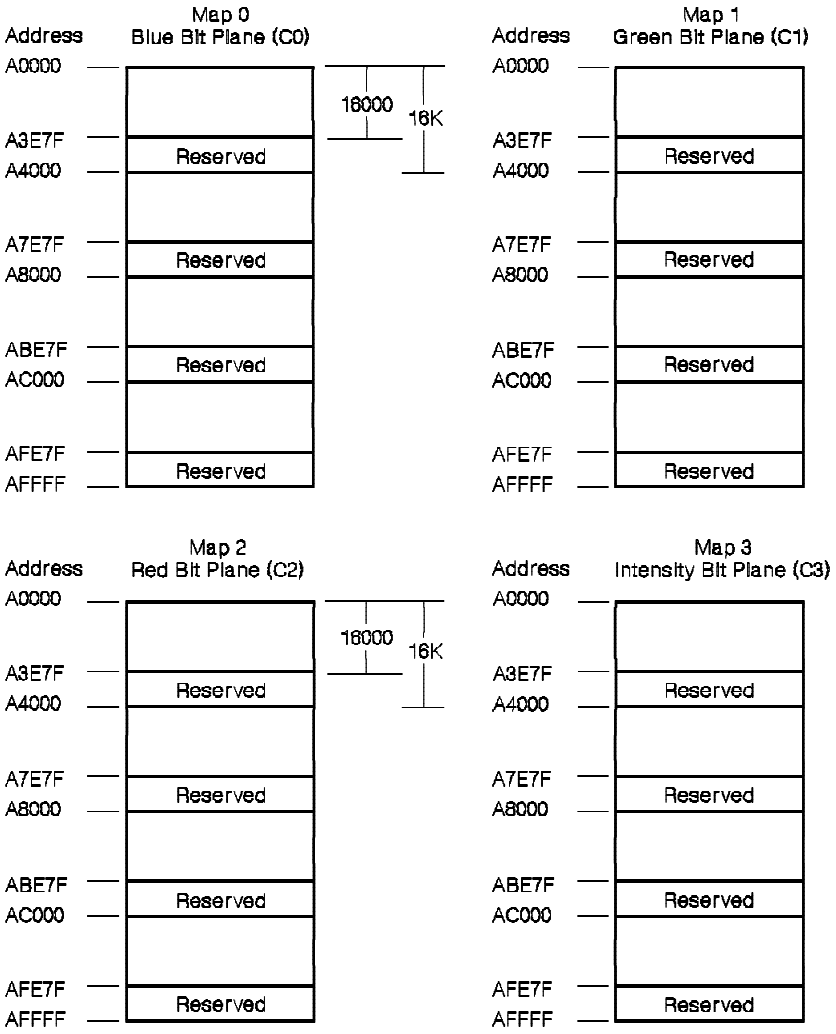
Mode Hex D


Address
Display Buffer
Storage Scheme
PEL
A0000 (A8000)
A1F3F (A9F3F)
A2000 (AA000)
A3F3F (ABF3F)
A4000 (AC000)
A5F3F (ADF3F)
A6000 (AE000)
A7F3F (AFF3F)
A7FFF (AFFFF)
Page 1 (5)
Reserved
Page 2 (6)
Reserved
Page 3 (7)
Reserved
Page 4 (8)
Reserved
8000
8K
1 2 3 4 5 6 7 8
C0
C1
C2
C3
MSB
LSB
• 4 bits per PEL
• 16 colors per PEL
• 1 bit from each bit plane (C3,C2,C1,C0) per PEL
• Format is first PEL in most significant byte of all 4 bit planes

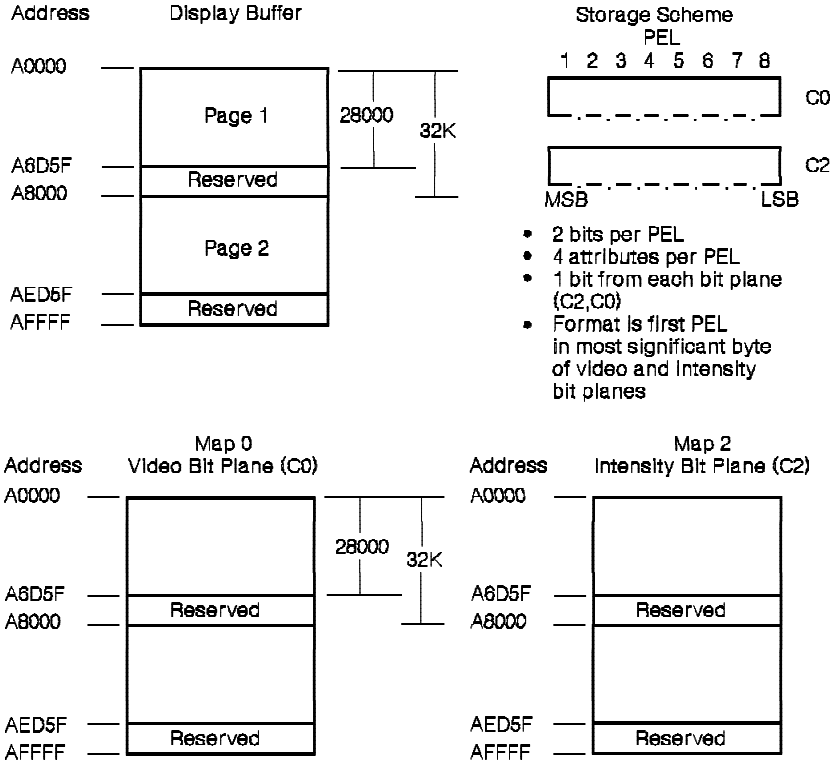

Map 0
Address
Blue Bit Plane (C0)
A0000 (A8000)
A1F3F (A9F3F)
A2000 (AA000)
A3F3F (ABF3F)
A4000 (AC000)
A5F3F (ADF3F)
A6000 (AE000)
A7F3F (AFF3F)
A7FFF (AFFFF)
Reserved
8000
8K
Map 1
Address
Green Bit Plane (C1)
Map 2
Address
Red Bit Plane (C2)
Map 3
Address
Intensity Bit Plane (C3)

Mode Hex E

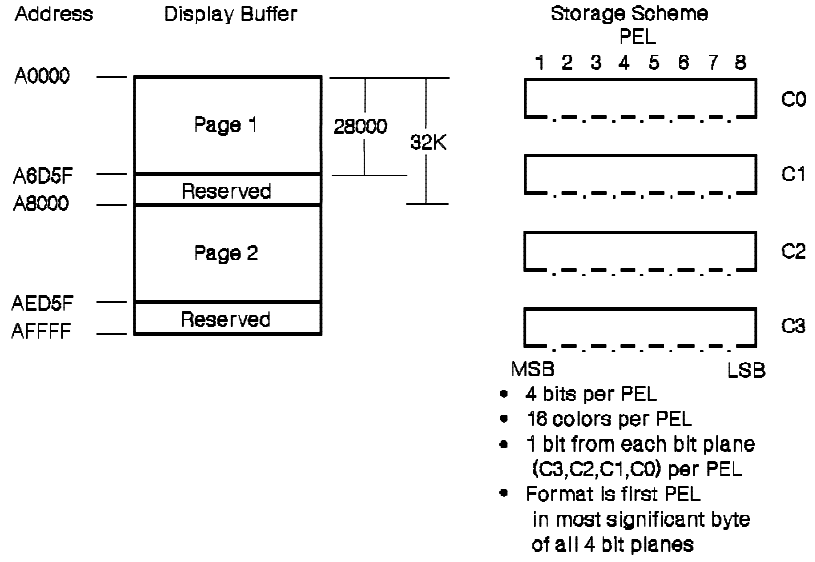

Address
Display Buffer
A0000
Page 1
16000
16K
A3E7F
Reserved
A4000
Page 2
A7E7F
Reserved
A8000
Page 3
ABE7F
Reserved
AC000
Page 4
AFE7F
Reserved
AFFFF
Storage Scheme
PEL
1 2 3 4 5 6 7 8
C0
C1
C2
C3
MSB
LSB
• 4 bits per PEL
• 16 colors per PEL
• 1 bit from each bit plane (C3,C2,C1,C0) per PEL
• Format is first PEL in most significant byte of all 4 bit planes


Map 0
Blue Bit Plane (C0)
Address
A0000
A3E7F
A4000
A7E7F
A8000
ABE7F
AC000
AFE7F
AFFFF
Reserved
16000
16K
Map 1
Green Bit Plane (C1)
Map 2
Red Bit Plane (C2)
Map 3
Intensity Bit Plane (C3)

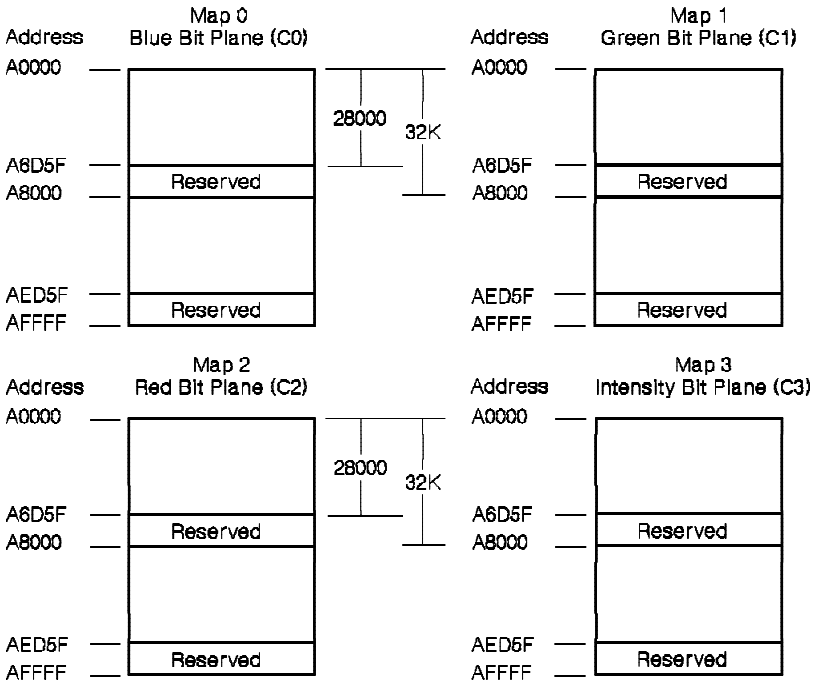
Mode Hex F


Address
Display Buffer
A0000
Page 1
28000
32K
A6D5F
Reserved
A8000
Page 2
AED5F
Reserved
AFFFF
Storage Scheme
PEL
1 2 3 4 5 6 7 8
C0
C2
MSB
LSB
• 2 bits per PEL
• 4 attributes per PEL
• 1 bit from each bit plane (C2,C0)
• Format is first PEL in most significant byte of video and intensity bit planes
Map 0
Address
Video Bit Plane (C0)
A0000
28000
32K
A6D5F
Reserved
A8000
AED5F
Reserved
AFFFF
Map 2
Address
Intensity Bit Plane (C2)
A0000
A6D5F
Reserved
A8000
AED5F
Reserved
AFFFF

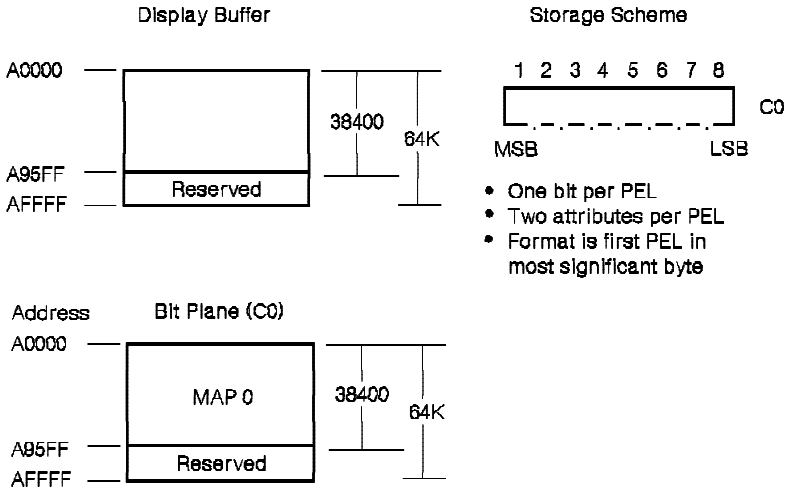
Mode Hex 10



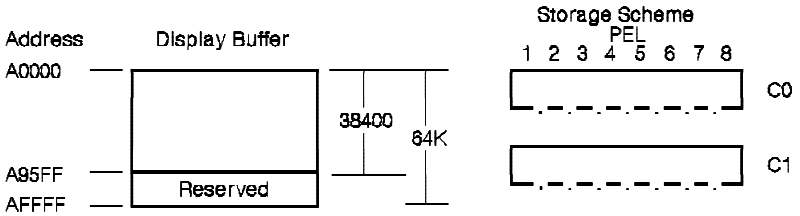
- 4 bits per PEL
- 16 colors per PEL
- 1 bit from each bit plane (C3,C2,C1,C0) per PEL
- Format is first PEL in most significant byte of all 4 bit planes



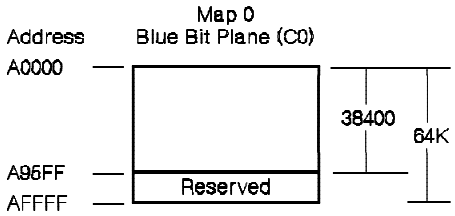
Mode Hex 11

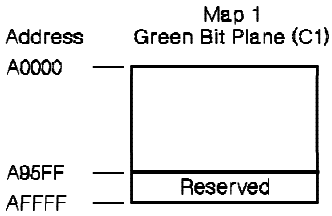

Display Buffer
A0000
A95FF
AFFFF
Reserved
38400
64K
Storage Scheme
1 2 3 4 5 6 7 8
C0
MSB
LSB
• One bit per PEL
• Two attributes per PEL
• Format is first PEL in most significant byte
Address
Bit Plane (C0)
A0000
MAP 0
A95FF
AFFFF
Reserved
38400
64K

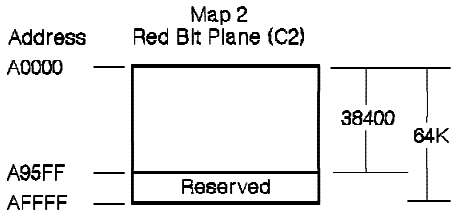
Mode Hex 12

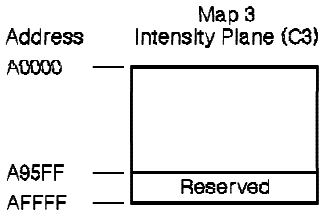


- 4 bits per PEL
- 16 colors per PEL
- 1 bit from each bit plane (C3,C2,C1,C0) per PEL
- Format is first PEL in most significant byte of all 4 bit planes

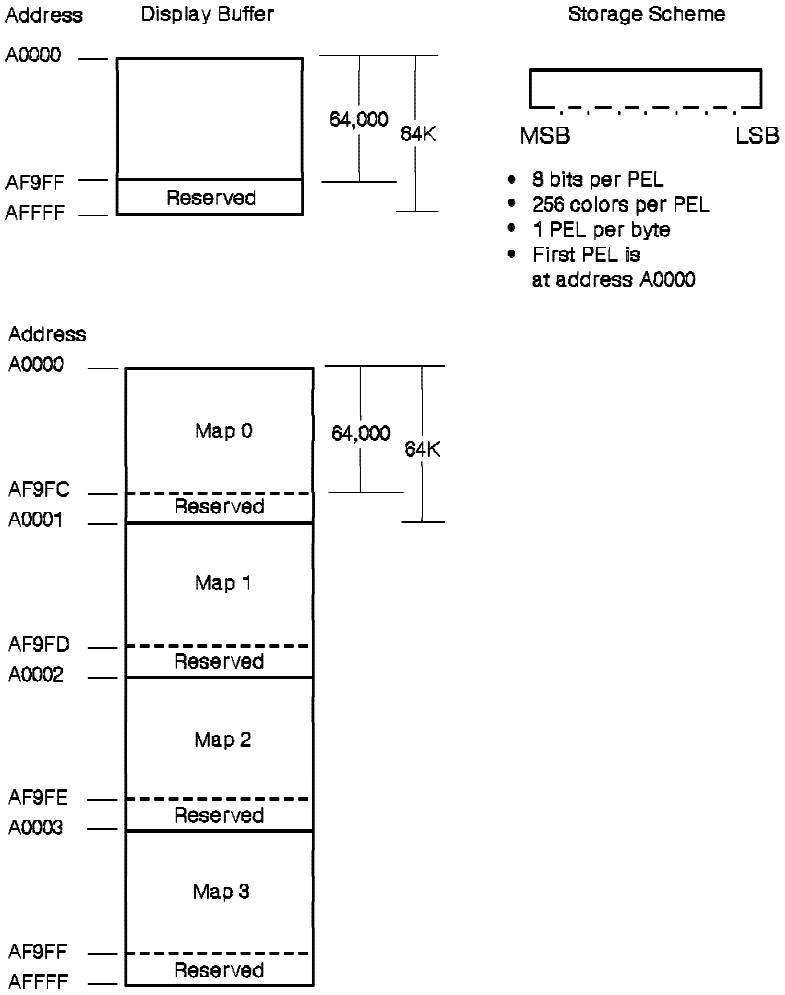








Mode Hex 13


Address
Display Buffer
A0000
AF9FF
AFFFF
Reserved
64,000
64K
Address
A0000
Map 0
AF9FC
Reserved
A0001
Map 1
AF9FD
Reserved
A0002
Map 2
AF9FE
Reserved
A0003
Map 3
AF9FF
Reserved
AFFFF
64,000
64K

Storage Scheme
MSB
LSB
• 8 bits per PEL
• 256 colors per PEL
• 1 PEL per byte
• First PEL is
at address A0000

Memory Operations

Memory operations consist of write and read operations.

Write Operations

When the system is writing to the display buffer, the maps are enabled by the logical decode of the memory address and the Map Mask register. The addresses used for video memory depend on the mode selected. The data flow for a system write operation is illustrated in the following figure.

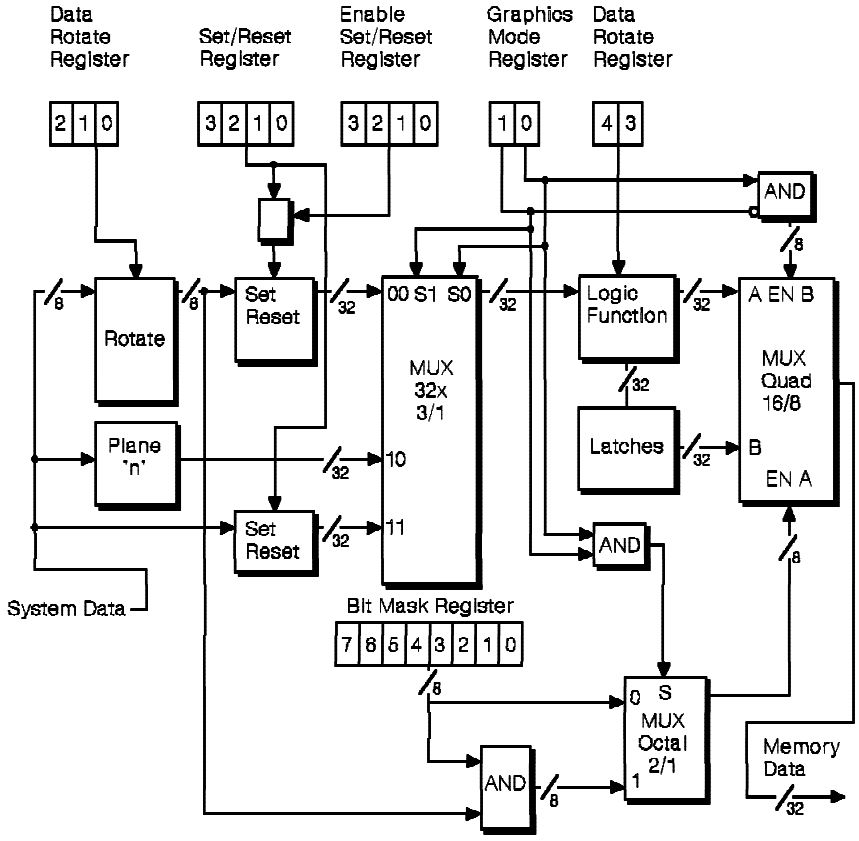


Figure 2-17. Data Flow for Write Operations

Read Operations

The two ways to read the video buffer are selected through the Graphics Mode register in the graphics controller. The mode 0 read operation returns the 8-bit value determined by the logical decode of the memory address and, if applicable, the Read Map Select register. The mode 1 read operation returns the 8-bit value resulting from the color compare operation controlled by the Color Compare and Color Don't Care registers. The data flow for the color compare operation is shown in the following figure.

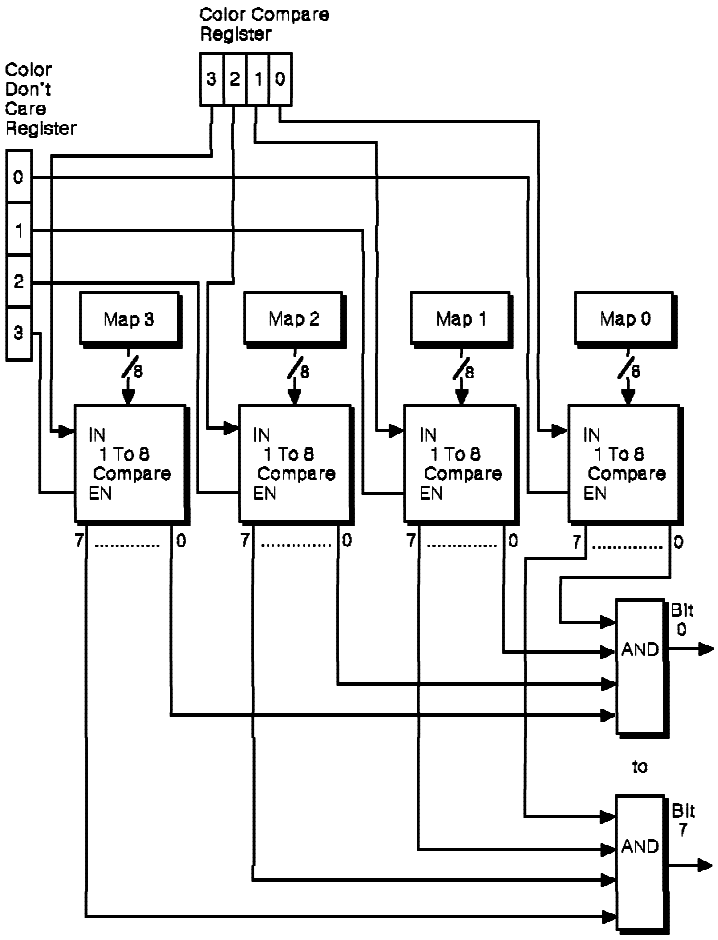


Figure 2-18. Color Compare Operations

Registers

There are six groups of registers in the video subsystem. All video registers are readable except the system data latches and the attribute address flip-flop. The following figure lists the register groups, their I/O addresses with the type of access (read or write), and page reference numbers.

The question mark in the address can be a hex B or D depending on the setting of the I/O address bit in the Miscellaneous Output register, described in “General Registers” on page 2-42.

Note: All registers in the video subsystem are read/write. The value of reserved bits in these registers must be preserved. Read the register first and change only the bits required.

Registers	R/W	Port Address	Page Reference
General Registers			2-42
Sequencer Registers			2-47
Address Register	R/W	03C4	
Data Registers	R/W	03C5	
CRT Controller Registers			2-55
Address Register	R/W	03?4	
Data Registers	R/W	03?5	
Graphics Controller Registers			2-78
Address Register	R/W	03CE	
Data Registers	R/W	03CF	
Attribute Controller Registers			2-89
Address Register	R/W	03C0	
Data Registers	W	03C0	
	R	03C1	
Video DAC Palette Registers			2-104
Write Address	R/W	03C8	
Read Address	W	03C7	
Data	R/W	03C9	
PEL Mask	R/W	03C6	

Figure 2-19. Video Subsystem Register Overview

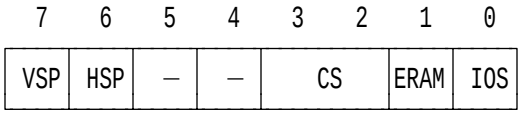
General Registers

Register	Read Address	Write Address
Miscellaneous Output Register	03CC	03C2
Input Status Register 0	03C2	–
Input Status Register 1	03?A	–
Feature Control Register	03CA	03?A
Video Subsystem Enable Register	03C3	03C3

Figure 2-20. General Registers

Miscellaneous Output Register

The read address for this register is hex 03CC and its write address is hex 03C2.




```
  — : Set to 0, Undefined on Read
VSP : Vertical Sync Polarity
HSP : Horizontal Sync Polarity
 CS : Clock Select
ERAM : Enable RAM
 IOS : I/O Address Select
```

Figure 2-21. Miscellaneous Output Register, Hex 03CC/03C2

The register fields are defined as follows:

VSP When set to 0, the Vertical Sync Polarity field (bit 7) selects a positive 'vertical retrace' signal. This bit works with bit 6 to determine the vertical size.

HSP When set to 0, the Horizontal Sync Polarity field (bit 6) selects a positive 'horizontal retrace' signal. Bits 7 and 6 select the vertical size as shown in the following figure.

Bits 7 6	Vertical Size
0 0	Reserved
0 1	400 lines
1 0	350 lines
1 1	480 lines

Figure 2-22. Display Vertical Size

CS The Clock Select field (bits 3, 2) selects the clock source according to the following figure. The external clock is driven through the auxiliary video extension. The input clock should be kept between 14.3 MHz and 28.4 MHz.

CS Field (binary)	Function
0 0	Selects 25.175 MHz clock for 640/320 Horizontal PELs
0 1	Selects 28.322 MHz clock for 720/360 Horizontal PELs
1 0	Selects External Clock
1 1	Reserved

Figure 2-23. Clock Select Definitions

ERAM When set to 0, the Enable RAM field (bit 1) disables address decode for the display buffer from the system.

IOS The I/O Address Select field (bit 0) selects the CRT controller addresses. When set to 0, this bit sets the CRT controller addresses to hex 03Bx and the address for the Input Status Register 1 to hex 03BA for compatibility with the monochrome adapter. When set to 1, this bit sets CRT controller addresses to hex 03Dx and the Input Status Register 1 address to hex 03DA for compatibility with the color/graphics adapter. The write addresses to the Feature Control register are affected in the same manner.

Input Status Register 0

The address for this read-only register is address hex 03C2. *Do not write to* this register.

7	6	5	4	3	2	1	0
CI	–	–	SS	–	–	–	–

– : Undefined on Read
CI : CRT Interrupt
SS : Switch Sense

Figure 2-24. Input Status Register 0, Hex 03C2

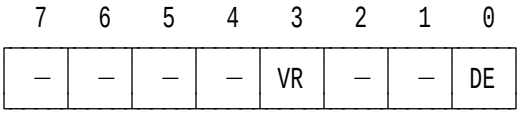
The register fields are defined as follows:

CI When the CRT Interrupt field (bit 7) is 1, a vertical retrace interrupt is pending.

SS BIOS uses the Switch Sense field (bit 4) in determining the type of display attached.

Input Status Register 1

The address for this read-only register is address hex 03DA or 03BA. *Do not write to* this register.



– : Undefined on Read
VR : Vertical Retrace
DE : Display Enable

Figure 2-25. Input Status Register 1, Hex 03DA/03BA

The register fields are defined as follows:

VR When the Vertical Retrace field (bit 3) is 1, it indicates a vertical retrace interval. This bit can be programmed, through the Vertical Retrace End register, to generate an interrupt at the start of the vertical retrace.

DE When the Display Enable field (bit 0) is 1, it indicates a horizontal or vertical retrace interval. This bit is the real-time status of the inverted 'display enable' signal. In the past, programs have used this status bit to restrict screen updates to the inactive display intervals to reduce screen flicker. The video subsystem is designed to eliminate this software requirement; screen updates may be made at any time without screen degradation.

Feature Control Register

The write address of this register is hex 03DA or 03BA; its read address is hex 03CA. All bits are reserved.

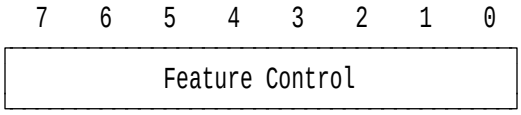


Figure 2-26. Feature Control Register, Hex 03DA/03BA and 03CA

Video Subsystem Enable Register

This register (hex 03C3) is reserved. To disable address decoding by the video subsystem, use BIOS INT 10 call, AH = hex 12, BL = hex 32.

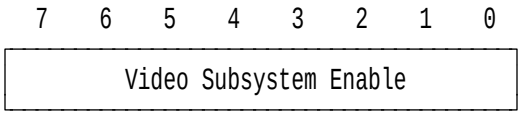


Figure 2-27. Video Subsystem Enable Register, Hex 03C3

Sequencer Registers

The Address register is at address hex 03C4 and the data registers are at address hex 03C5. All registers within the sequencer are read/write.

Register	Index (Hex)
Sequencer Address	–
Reset	00
Clocking Mode	01
Map Mask	02
Character Map Select	03
Memory Mode	04

Figure 2-28. Sequencer Registers

Sequencer Address Register

The Address register is at address hex 03C4. This register is loaded with an index value that points to the desired sequencer data register.

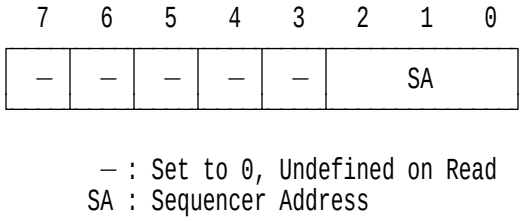


Figure 2-29. Sequencer Address Register

The register field is defined as follows:

SA The Sequencer Address field (bits 2– 0) contains the index value that points to the data register to be accessed.

Reset Register

This read/write register has an index of hex 00; its address is hex 03C5.

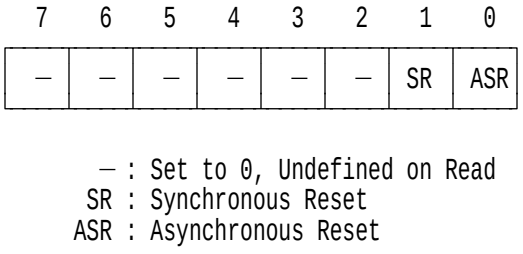


Figure 2-30. Reset Register, Index Hex 00

The register fields are defined as follows:

SR When set to 0, the Synchronous Reset field (bit 1) commands the sequencer to synchronously clear and halt. Bits 1 and 0 must be 1 to allow the sequencer to operate. To prevent the loss of data, bit 1 must be set to 0 during the active display interval before changing the clock selection. The clock is changed through the Clocking Mode register or the Miscellaneous Output register.

ASR When set to 0, the Asynchronous Reset field (bit 0) commands the sequencer to asynchronously clear and halt. Resetting the sequencer with this bit can cause loss of video data.

Clocking Mode Register

This read/write register has an index of hex 01; its address is hex 03C5.

7	6	5	4	3	2	1	0
–	–	SO	SH4	DC	SL	1	D89

```
  – : Set to 0, Undefined on Read
  1 : Set to 1, Undefined on Read
 SO : Screen Off
SH4 : Shift 4
 DC : Dot Clock
 SL : Shift Load
D89 : 8/9 Dot Clocks
```

Figure 2-31. Clocking Mode Register, Index Hex 01

The register fields are defined as follows:

SO When set to 1, the Screen Off field (bit 5) turns off the display and assigns maximum memory bandwidth to the system. Although the display is blanked, the synchronization pulses are maintained. This bit can be used for rapid full-screen updates.

SH4 When the Shift 4 field (bit 4) and Shift Load field (bit 2) are set to 0, the video serializers are loaded every character clock. When the Shift 4 field is set to 1, the video serializers are loaded every fourth character clock, which is useful when 32 bits are fetched per cycle and chained together in the shift registers.

Extended Graphics mode behaves as if this bit is set to 0; therefore, programs should set it to 0.

DC When set to 0, the Dot Clock field (bit 3) selects the normal dot clocks derived from the sequencer master clock input. When set to 1, the master clock is divided by 2 to generate the dot clock. All other timings are affected because they are derived from the dot clock. The dot clock divided by 2 is used for 320 and 360 horizontal PEL modes.

SL When the Shift Load field (bit 2) and Shift 4 field (bit 4) are set to 0, the video serializers are loaded every character clock. When the Shift Load field (bit 2) is set to 1, the video serializers are loaded every other character clock, which is useful when 16 bits are fetched per cycle and chained together in the shift registers.

Extended Graphics mode behaves as if this bit is set to 0; therefore, programs should set it to 0.

D89 When set to 0, the 8/9 Dot Clocks field (bit 0) directs the sequencer to generate character clocks 9 dots wide; when set to 1, it directs the sequencer to generate character clocks 8 dots wide. The 9-dot mode is for alphanumeric modes 0+, 1+, 2+, 3+, 7, and 7+ only; the 9th dot equals the 8th dot for ASCII codes hex C0 through DF. All other modes must use 8 dots per character clock. (See the Enable Line Graphics Character Code field in the Attribute Mode Control register on page 2-92.)

Map Mask Register

This read/write register has an index of hex 02; its address is hex 03C5.

7	6	5	4	3	2	1	0
–	–	–	–	M3E	M2E	M1E	M0E

– : Set to 0, Undefined on Read
M3E : Map 3 Enable
M2E : Map 2 Enable
M1E : Map 1 Enable
M0E : Map 0 Enable

Figure 2-32. Map Mask Register, Index Hex 02

The register fields are defined as follows:

M3E, M2E, M1E, M0E

When set to 1, the map enable fields (bits 3, 2, 1, and 0) enable system access to the corresponding map. If all maps are enabled (chain 4 mode), the system can write its 8-bit value to all four maps in a single memory cycle. This substantially reduces the system overhead during display updates in graphics modes.

Data scrolling operations can be enhanced by enabling all maps and writing the display buffer address with the data stored in the system data latches. This is a read-modify-write operation.

When access to odd or even maps (odd/even modes) are selected, maps 0 and 1 and maps 2 and 3 should have the same map mask value.

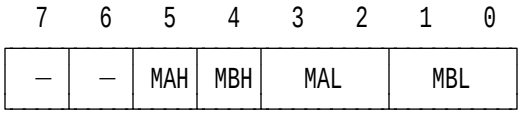
When chain 4 mode is selected, all maps should be enabled.

Character Map Select Register

This register has an index of hex 03; its address is hex 03C5. In alphanumeric modes, bit 3 of the attribute byte normally defines the foreground intensity. This bit can be redefined as a switch between character sets, allowing 512 displayable characters. To enable this feature:

1. Set the extended memory bit in the Memory Mode register (index hex 04) to 1.
2. Select different values for character map A and character map B.

This function is supported by BIOS and is a function call within the character generator routines.



– : Set to 0, Undefined on Read
MAH : Character Map A Select (MSB)
MBH : Character Map B Select (MSB)
MAL : Character Map A Select (LS bits)
MBL : Character Map B Select (LS bits)

Figure 2-33. Character Map Select Register, Index Hex 03

The register fields are defined as follows:

MAH The Character Map A Select field (bit 5) is the most-significant bit for selecting the location of character map A.

MBH The Character Map B Select field (bit 4) is the most-significant bit for selecting the location of character map B.

MAL The Character Map A Select field (bits 3, 2) and Character Map A Select field (bit 5) select the location of character map A. Map A is the area of map 2 containing the character font table used to generate characters when attribute bit 3 is set to 1. The selection is shown in the following figure.

Bits 5 3 2	Map Selected	Table Location
0 0 0	0	1st 8KB of Map 2
0 0 1	1	3rd 8KB of Map 2
0 1 0	2	5th 8KB of Map 2
0 1 1	3	7th 8KB of Map 2
1 0 0	4	2nd 8KB of Map 2
1 0 1	5	4th 8KB of Map 2
1 1 0	6	6th 8KB of Map 2
1 1 1	7	8th 8KB of Map 2

Figure 2-34. Character Map Select A

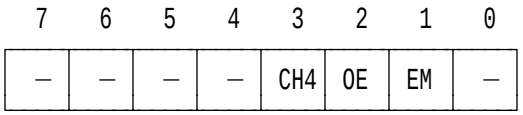
MBL The Character Map B Select field (bits 1, 0) and Character Map B Select field (bit 4) select the location of character map B. Map B is the area of map 2 containing the character font table used to generate characters when attribute bit 3 is set to 0. The selection is shown in the following figure.

Bits 4 1 0	Map Selected	Table Location
0 0 0	0	1st 8KB of Map 2
0 0 1	1	3rd 8KB of Map 2
0 1 0	2	5th 8KB of Map 2
0 1 1	3	7th 8KB of Map 2
1 0 0	4	2nd 8KB of Map 2
1 0 1	5	4th 8KB of Map 2
1 1 0	6	6th 8KB of Map 2
1 1 1	7	8th 8KB of Map 2

Figure 2-35. Character Map Select B

Memory Mode Register

This register has an index of hex 04; its address is hex 03C5.



– : Set to 0, Undefined on Read
CH4 : Chain 4
OE : Odd/Even
EM : Extended Memory

Figure 2-36. Memory Mode Register, Index Hex 04

The register fields are defined as follows:

CH4 The Chain 4 field (bit 3) controls the map selected during system read operations. When set to 0, this bit enables system addresses to sequentially access data within a bit map by using the Map Mask register. When set to 1, this bit causes the 2 low-order bits to select the map accessed as shown in the following figure.

Address Bits A1 A0	Map Selected
0 0	0
0 1	1
1 0	2
1 1	3

Figure 2-37. Map Selection, Chain 4

OE When the Odd/Even field (bit 2) is set to 0, even system addresses access maps 0 and 2, while odd system addresses access maps 1 and 3. When set to 1, system addresses sequentially access data within a bit map, and the maps are accessed according to the value in the Map Mask register (hex 02).

EM When set to 1, the Extended Memory field (bit 1) enables the video memory from 64KB to 256KB. This bit must be set to 1 to enable the character map selection described for the previous register.

CRT Controller Registers

A data register is accessed by writing its index to the Address register at address hex 03D4 or 03B4, and then writing the data to the access port at address hex 03D5 or 03B5. The I/O address used depends on the setting of the I/O address select bit (bit 0) in the Miscellaneous Output register, which is described in “General Registers” on page 2-42. The following figure shows the variable part of the address as a question mark.

Note: When modifying a register, the setting of reserved bits must be preserved. Read the register first and change only the bits required.

Register Name	Address (Hex)	Index (Hex)
Address	03?4	–
Horizontal Total	03?5	00
Horizontal Display-Enable End	03?5	01
Start Horizontal Blanking	03?5	02
End Horizontal Blanking	03?5	03
Start Horizontal Retrace Pulse	03?5	04
End Horizontal Retrace	03?5	05
Vertical Total	03?5	06
Overflow	03?5	07
Preset Row Scan	03?5	08
Maximum Scan Line	03?5	09
Cursor Start	03?5	0A
Cursor End	03?5	0B
Start Address High	03?5	0C
Start Address Low	03?5	0D
Cursor Location High	03?5	0E
Cursor Location Low	03?5	0F
Vertical Retrace Start	03?5	10
Vertical Retrace End	03?5	11
Vertical Display-Enable End	03?5	12
Offset	03?5	13
Underline Location	03?5	14
Start Vertical Blanking	03?5	15
End Vertical Blanking	03?5	16
CRT Mode Control	03?5	17
Line Compare	03?5	18

Index values not listed are reserved.

Figure 2-38. CRT Controller Registers

Address Register

This register is at address hex 03B4 or 03D4, and is loaded with an index value that points to the data registers within the CRT controller.

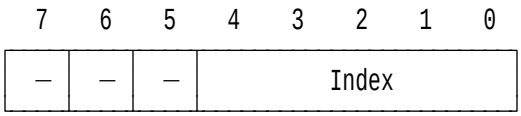


Figure 2-39. CRT Controller Address Register, Hex 03B4/03D4

The register field is defined as follows:

Index This field (bits 4– 0) is the index that points to the data register accessed through address hex 03D5 or 03B5.

Horizontal Total Register

This register has an index of hex 00; its address is hex 03D5 or 03B5.

The Horizontal Total register (bits 7– 0) defines the total number of characters in the horizontal scan interval including the retrace time. The value directly controls the period of the 'horizontal retrace' signal. A horizontal character counter in the CRT controller counts the character clock inputs; comparators are used to compare the register value with the horizontal width of the character to provide horizontal timings. All horizontal and vertical timings are based on this register.

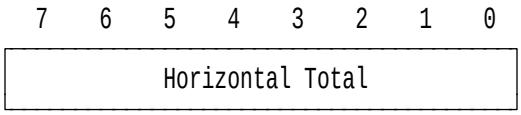


Figure 2-40. Horizontal Total Register, Index Hex 00

The value contained in the register is the total number of characters minus 5.

Horizontal Display-Enable End Register

This register has an index of hex 01; its address is hex 03D5 or 03B5.

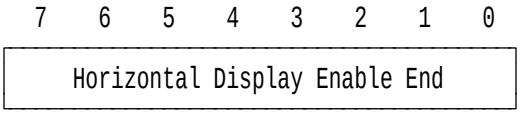


Figure 2-41. Horizontal Display Enable-End Register, Index Hex 01

The Horizontal Display-Enable End register (bits 7– 0) defines the length of the 'horizontal display-enable' signal and determines the number of character positions per horizontal line. The value in this register is the total number of displayed characters minus 1.

Start Horizontal Blanking Register

This register has an index of hex 02; its address is hex 03D5 or 03B5.

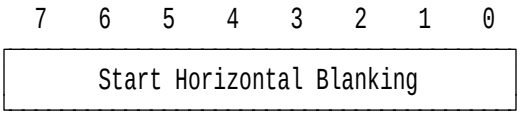
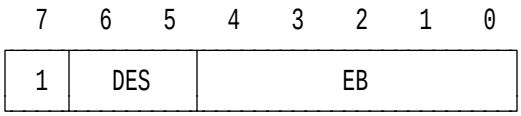


Figure 2-42. Start Horizontal Blanking Register, Index Hex 02

The value in the Start Horizontal Blanking register (bits 7– 0) is the horizontal character count at which the 'horizontal blanking' signal goes active.

End Horizontal Blanking Register

This register has an index of hex 03; its address is hex 03D5 or 03B5. It determines when the 'horizontal blanking' signal will go active.




```
  1 : Set to 1, Undefined on Read
DES : Display Enable Skew Control
 EB : End Blanking
```

Figure 2-43. End Horizontal Blanking Register, Index Hex 03

The register fields are defined as follows:

DES The Display Enable Skew Control field (bits 6, 5) determines the amount of skew of the 'display enable' signal. This skew control is needed to provide sufficient time for the CRT controller to read a character and attribute code from the video buffer, gain access to the character generator, and go through the Horizontal PEL Panning register in the attribute controller. Each access requires the 'display enable' signal to be skewed one character clock so that the video output is synchronized with the horizontal and vertical retrace signals. The skew values are shown in the following figure.

DES Field (binary)	Amount of Skew
0 0	No character clock skew
0 1	One character clock skew
1 0	Two character clock skew
1 1	Three character clock skew

Figure 2-44. Display Enable Skew

Note: Character skew is not adjustable on the Type 2 video and the bits are ignored; however, programs should set these bits for the appropriate skew to maintain compatibility.

EB The End Blanking field (bits 4– 0) contains the 5 low-order bits of a 6-bit value that is compared with the value in the Start Horizontal Blanking register to determine when the 'horizontal blanking' signal goes inactive. The most-significant bit is bit 7 in the End Horizontal Retrace register (index hex 05).

To program these bits for a signal width of W, the following algorithm is used: the width W, in character clock units, is added to the value from the Start Horizontal Blanking register. The 6 low-order bits of the result are the 6-bit value programmed.

Start Horizontal Retrace Pulse Register

This register has an index of hex 04; its address is hex 03D5 or 03B5.

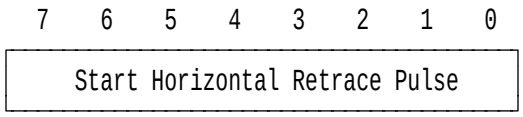
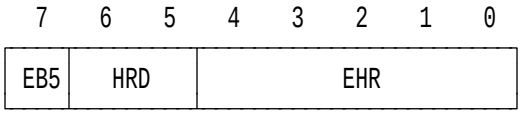


Figure 2-45. Start Horizontal Retrace Pulse Register, Index Hex 04

The Start Horizontal Retrace Pulse register (bits 7– 0) is used to center the screen horizontally by specifying the character position where the 'horizontal retrace' signal goes active.

End Horizontal Retrace Register

This register has an index of hex 05; its address is hex 03D5 or 03B5.



EB5 : End Horizontal Blanking, Bit 5
HRD : Horizontal Retrace Delay
EHR : End Horizontal Retrace

Figure 2-46. End Horizontal Retrace Register, Index Hex 05

The register fields are defined as follows:

EB5 The End Horizontal Blanking, Bit 5 field (bit 7) is the most-significant bit of the end horizontal blanking value in the End Horizontal Blanking register (index hex 03).

HRD The Horizontal Retrace Delay field (bits 6, 5) controls the skew of the 'horizontal retrace' signal. The value of this field is the amount of skew provided (from 0 to 3 character clock units). For certain modes, the 'horizontal retrace' signal takes up the entire blanking interval. Some internal timings are generated by the falling edge of the 'horizontal retrace' signal. To ensure that the signals are latched properly, the 'retrace' signal is started before the end of the 'display enable' signal and then skewed several character clock times to provide the proper screen centering.

EHR The End Horizontal Retrace field (bits 4– 0) is compared with the Start Horizontal Retrace register to give a horizontal character count at which the 'horizontal retrace' signal goes inactive.

To program these bits with a signal width of W, the following algorithm is used: the width W, in character clock units, is added to the value in the Start Retrace register. The 5 low-order bits of the result are the 5-bit value programmed.

Vertical Total Register

This register has an index of hex 06; its address is hex 03D5 or 03B5.

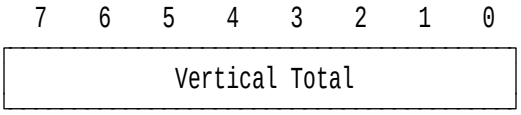


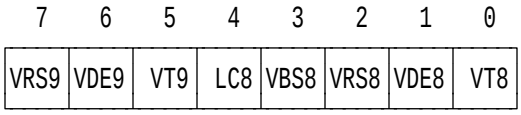
Figure 2-47. Vertical Total Register, Index Hex 06

The Vertical Total register (bits 7– 0) contains the 8 low-order bits of a 10-bit vertical total. The value for the vertical total is the number of horizontal raster scans on the display, including vertical retrace, minus 2. This value determines the period of the 'vertical retrace' signal.

Bits 8 and 9 are in the Overflow register (index hex 07).

Overflow Register

This register has an index of hex 07; its address is hex 03D5 or 03B5.




```
VRS9 : Vertical Retrace Start, Bit 9
VDE9 : Vertical Display Enable End, Bit 9
 VT9 : Vertical Total, Bit 9
 LC8 : Line Compare, Bit 8
VBS8 : Vertical Blanking Start, Bit 8
VRS8 : Vertical Retrace Start, Bit 8
VDE8 : Vertical Display Enable End, Bit 8
 VT8 : Vertical Total, Bit 8
```

Figure 2-48. CRT Overflow Register, Index Hex 07

The register fields are defined as follows:

VRS9 This is bit 9 of the Vertical Retrace Start register (index hex 10).

VDE9 This is bit 9 of the Vertical Display-Enable End register (index hex 12).

VT9 This is bit 9 of the Vertical Total register (index hex 06).

LC8 This is bit 8 of the Line Compare register (index hex 18).

VBS8 This is bit 8 of the Start Vertical Blanking register (index hex 15).

VRS8 This is bit 8 of the Vertical Retrace Start register (index hex 10).

VDE8 This is bit 8 of the Vertical Display-Enable End register (index hex 12).

VT8 This is bit 8 of the Vertical Total register (index hex 06).

Preset Row Scan Register

This register has an index of hex 08; its address is hex 03D5 or 03B5.

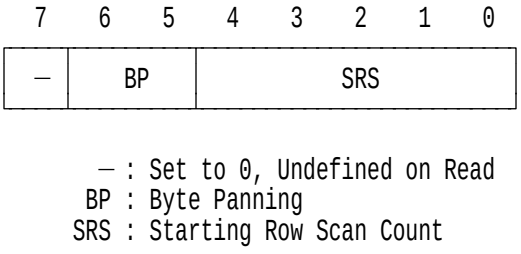


Figure 2-49. Preset Row Scan Register, Index Hex 08

The register fields are defined as follows:

BP The Byte Panning field (bits 6, 5) controls byte panning in multiple shift modes. (BIOS modes do not use multiple shift operation.) These bits are used in PEL-panning operations, and should normally be set to 0.

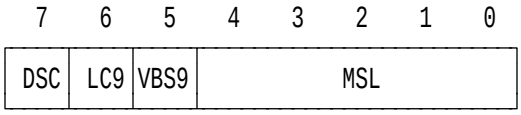
Extended Graphics mode behaves as if these bits are set to 0; therefore, programs should set it to 0.

SRS The Starting Row Scan Count field (bits 4– 0) specifies the row scan count for the row starting after a vertical retrace. The row scan counter is incremented every horizontal retrace time until the maximum row scan occurs. When the maximum row scan is reached, the row scan counter is cleared (not preset).

Note: The CRT controller latches the start address at the start of the vertical retrace. These register values should be loaded during the active display time.

Maximum Scan Line Register

This register has an index of hex 09; its address is hex 03D5 or 03B5.



DSC : 200 to 400 Line Conversion (Double Scanning)
LC9 : Line Compare, Bit 9
VBS9 : Start Vertical Blanking, Bit 9
MSL : Maximum Scan Line

Figure 2-50. Maximum Scan Line Register, Index Hex 09

The register fields are defined as follows:

DSC When the 200 to 400 Line Conversion field (bit 7) is set to 1, 200-scan-line video data is converted to 400-scan-line output. To do this, the clock in the row scan counter is divided by 2, which allows the 200-line modes to be displayed as 400 lines on the display (this is called double scanning; each line is displayed twice). When set to 0, the clock to the row scan counter is equal to the horizontal scan rate.

LC9 The Line Compare, Bit 9 field (bit 6) is bit 9 of the Line Compare register (index hex 18).

VBS9 The Start Vertical Blanking, Bit 9 field (bit 5) is bit 9 of the Start Vertical Blanking register (index hex 15).

MSL The Maximum Scan Line field (bits 4– 0) specifies the number of scan lines per character row. The value of this field is the maximum row scan number minus 1.

Cursor Start Register

This register has an index of hex 0A; its address is hex 03D5 or 03B5.

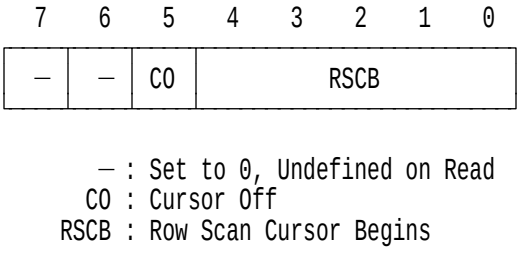


Figure 2-51. Cursor Start Register, Index Hex 0A

The register fields are defined as follows:

CO When the Cursor Off field (bit 5) is set to 1, the cursor is disabled.

RSCB The Row Scan Cursor Begins field (bits 4– 0) specifies the row within the character box where the cursor begins. The value of this field is the first line of the cursor minus 1. When this value is greater than that in the Cursor End register, no cursor is displayed.

Cursor End Register

This register has an index of hex 0B; its address is hex 03D5 or 03B5.

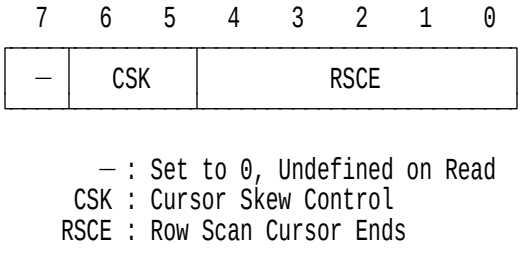


Figure 2-52. Cursor End Register, Index Hex 0B

The register fields are defined as follows:

CSK The Cursor Skew Control field (bits 6, 5) controls the skew of the cursor. The skew value delays the cursor by the selected number of character clocks from 0 to 3. For example, a skew of 1 moves the cursor right one position on the screen.

RSCE The Row Scan Cursor Ends field (bits 4– 0) specifies the row within the character box where the cursor ends. If this value is less than that in the Cursor Start register, no cursor is displayed.

Start Address High Register

This register has an index of hex 0C; its address is hex 03D5 or 03B5.

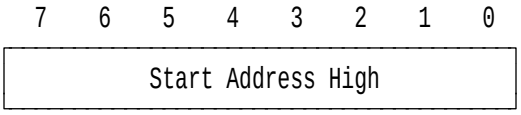


Figure 2-53. Start Address High Register, Index Hex 0C

The Start Address High register (bits 7– 0) contains the 8 high-order bits of a 16-bit value that specifies the starting address for the regenerative buffer. The start address points to the first address after the vertical retrace on each screen refresh.

Note: The CRT controller latches the start address at the start of the vertical retrace. These register values should be loaded during the active display time.

Start Address Low Register

This register has an index of hex 0D; its address is hex 03D5 or 03B5.

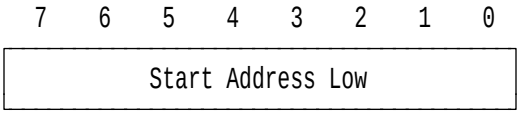


Figure 2-54. Start Address Low Register, Index Hex 0D

The Start Address Low register (bits 7– 0) contains the 8 low-order bits of the starting address for the regenerative buffer.

Cursor Location High Register

This register has an index of hex 0E; its address is hex 03D5 or 03B5.

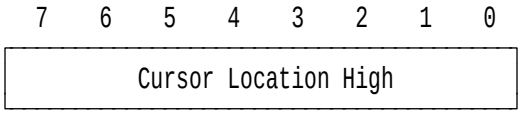


Figure 2-55. Cursor Location High Register, Index Hex 0E

The Cursor Location High register (bits 7– 0) contains the 8 high-order bits of the 16-bit cursor location.

Cursor Location Low Register

This register has an index of hex 0F; its address is hex 03D5 or 03B5.

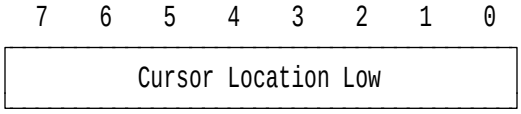


Figure 2-56. Cursor Location Low Register, Index Hex 0F

The Cursor Location Low register (bits 7– 0) contains the 8 low-order bits of the cursor location.

Vertical Retrace Start Register

This register has an index of hex 10; its address is hex 03D5 or 03B5.

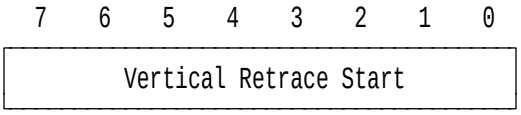
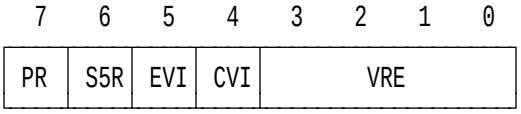


Figure 2-57. Vertical Retrace Start Register, Index Hex 10

The Vertical Retrace Start register (bits 7– 0) contains the 8 low-order bits of the 9-bit start position for the 'vertical retrace' signal; it is programmed in horizontal scan lines. Bit 8 is in the Overflow register (index hex 07).

Vertical Retrace End Register

This register has an index of hex 11; its address is hex 03D5 or 03B5.



PR : Protect Registers 0-7
S5R : Select 5 Refresh Cycles
EVI : Enable Vertical Interrupt
CVI : Clear Vertical Interrupt
VRE : Vertical Retrace End

Figure 2-58. Vertical Retrace End Register, Index Hex 11

The register fields are defined as follows:

PR When the Protect Registers 0– 7 field (bit 7) is set to 1, write access to the CRT controller registers at index 00 through 07 is disabled. The line compare bit in the Overflow register (index hex 07) is not protected.

S5R When the Select 5 Refresh Cycles field (bit 6) is set to 1, five memory refresh cycles per horizontal line are generated. When set to 0, three refresh cycles are selected. Selecting five refresh cycles allows use of the VGA chip with 15.75 kHz displays. This bit should be set to 0 for supported operations. It is set to 0 by a BIOS mode set, a reset, or a power on.

EVI When the Enable Vertical Interrupt field (bit 5) is set to 0, it enables a vertical retrace interrupt. The vertical retrace interrupt is IRQ2. This interrupt level can be shared, therefore, to determine whether the video generated the interrupt, check the CRT interrupt bit in Input Status Register 0.

CVI When the Clear Vertical Interrupt field (bit 4) is set to 0, it clears a vertical retrace interrupt. At the end of the active vertical display time, a flip-flop is set to indicate an interrupt. An interrupt handler resets this flip-flop by first setting this bit to 0, then resetting it to 1.

VRE The Vertical Retrace Start register is compared with the 4 bits in the Vertical Retrace End field (bits 3– 0) to determine where the ‘vertical retrace’ signal goes inactive. It is programmed in units of horizontal scan lines. To program these bits with a signal width of W, the following algorithm is used: the width W, in horizontal scan units, is added to the value in the Start Vertical Retrace register. The 4 low-order bits of the result are the 4-bit value programmed.

Vertical Display-Enable End Register

This register has an index of hex 12; its address is hex 03D5 or 03B5.

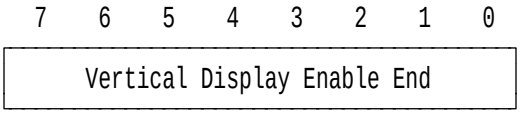


Figure 2-59. Vertical Display-Enable End Register, Index Hex 12

The Vertical Display-Enable End register (bits 7– 0) contains the 8 low-order bits of a 10-bit value that defines the vertical-display-enable end position. The 2 high-order bits are contained in the Overflow register (index hex 07). The 10-bit value is equal to the total number of scan lines minus 1.

Offset Register

This register has an index of hex 13; its address is hex 03D5 or 03B5.

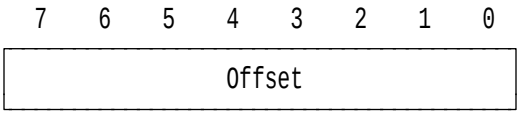
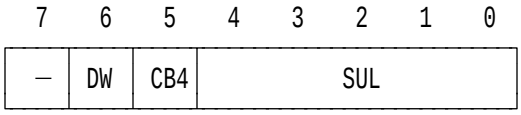


Figure 2-60. Offset Register, Index Hex 13

The Offset register (bits 7– 0) specifies the logical line width of the screen. The starting memory address for the next character row is larger than the current character row by 2 or 4 times the value of these bits. Depending on the method of clocking the CRT controller, this address is either a word or doubleword address.

Underline Location Register

This register has an index of hex 14; its address is hex 03D5 or 03B5.



– : Set to 0, Undefined on Read
DW : Doubleword Mode
CB4 : Count By 4
SUL : Start Underline

Figure 2-61. Underline Location Register, Index Hex 14

The register fields are defined as follows:

DW When the Doubleword Mode field (bit 6) is set to 1, memory addresses are doubleword addresses. See the description of the word/byte mode bit (bit 6) in the CRT Mode Control register on page 2-74.

CB4 When the Count By 4 field (bit 5) is set to 1, the memory-address counter is clocked with the character clock divided by 4, which is used when doubleword addresses are used.

SUL The Start Underline field (bits 4– 0) specifies the horizontal scan line of a character row on which an underline occurs. The value programmed is the scan line desired minus 1.

Start Vertical Blanking Register

This register has an index of hex 15; its address is hex 03D5 or 03B5.

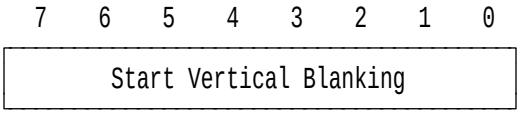


Figure 2-62. Start Vertical Blanking Register, Index Hex 15

The Start Vertical Blanking register (bits 7– 0) contains the 8 low-order bits of a 10-bit value that specifies the starting location for the 'vertical blanking' signal. Bit 8 is in the Overflow register (index hex 07) and bit 9 is in the Maximum Scan Line register (index hex 09). The 10-bit value is the horizontal scan line count at which the 'vertical blanking' signal becomes active minus 1.

End Vertical Blanking Register

This register has an index of hex 16; its address is hex 03D5 or 03B5.

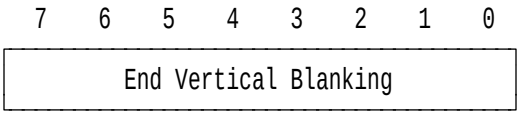


Figure 2-63. End Vertical Blanking Register, Index Hex 16

The End Vertical Blanking register (bits 7– 0) specifies the horizontal scan count at which the 'vertical blanking' signal becomes inactive. The register is programmed in units of the horizontal scan line.

To program these bits with a 'vertical blanking' signal of width W, the following algorithm is used: the width W, in horizontal scan line units, is added to the value in the Start Vertical Blanking register minus 1. The 8 low-order bits of the result are the 8-bit value programmed.

CRT Mode Control Register

This register has an index of hex 17; its address is hex 03D5 or 03B5.

7	6	5	4	3	2	1	0
RST	WB	ADW	—	CB2	HRS	SRC	CMS0

```
  — : Set to 0, Undefined on Read
RST : Hardware Reset
 WB : Word/Byte Mode
ADW : Address Wrap
CB2 : Count By Two
HRS : Horizontal Retrace Select
SRC : Select Row Scan Counter
CMS0 : CMS 0
```

Figure 2-64. CRT Mode Control Register, Index Hex 17

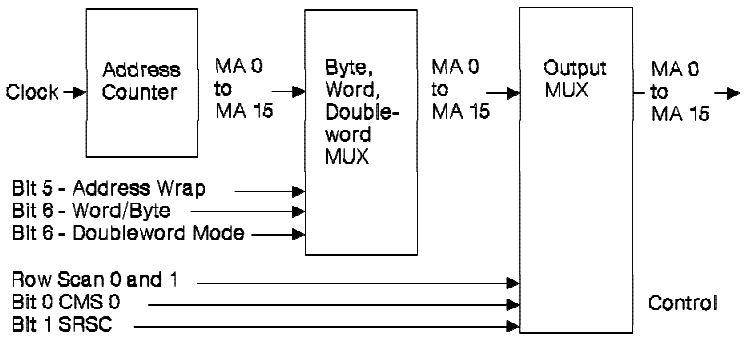
The register fields are defined as follows:

RST When the Hardware Reset field (bit 7) is set to 0, this bit disables the horizontal and vertical retrace signals and forces them to an inactive level. When set to 1, this bit enables the horizontal and vertical retrace signals. This bit does not reset any other registers or signal outputs.

WB When the Word/Byte Mode field (bit 6) is set to 0, the word mode is selected. The word mode shifts the memory-address counter bits down 1 bit; the most-significant bit of the counter appears on the least-significant bit of the memory address outputs.

The doubleword bit in the Underline Location register (index hex 14) also controls the addressing. When the doubleword bit is 0, the word/byte bit selects the mode. When the doubleword bit is set to 1, the addressing is shifted by 2 bits.

When the Word/Byte Mode field is set to 1, it selects the byte address mode. See the following figure for address output details.



Memory Address Outputs	Modes of Addressing		
	Byte	Word	Doubleword
MA 0	MA 0	MA 15 or 13	MA 12
MA 1	MA 1	MA 0	MA 13
MA 2	MA 2	MA 1	MA 0
MA 3	MA 3	MA 2	MA 1
MA 4	MA 4	MA 3	MA 2
MA 5	MA 5	MA 4	MA 3
MA 6	MA 6	MA 5	MA 4
MA 7	MA 7	MA 6	MA 5
MA 8	MA 8	MA 7	MA 6
MA 9	MA 9	MA 8	MA 7
MA 10	MA 10	MA 9	MA 8
MA 11	MA 11	MA 10	MA 9
MA 12	MA 12	MA 11	MA 10
MA 13	MA 13	MA 12	MA 11
MA 14	MA 14	MA 13	MA 12
MA 15	MA 15	MA 14	MA 13

Figure 2-65. CRT Memory Address Mapping

ADW The Address Wrap field (bit 5) selects the memory-address bit, bit MA 13 or MA 15, that appears on the output pin MA 0 in the word address mode. If VGA is not in the word address mode, bit 0 from the address counter appears on the output pin, MA 0.

When set to 1, the Address Wrap field bit selects MA 15. In odd/even mode, this bit should be set to 1 because 256KB of video memory is installed on the system board. (Bit MA 13 is selected in applications where only 64KB is present. This function maintains compatibility with the IBM Color/Graphics Monitor Adapter.)

CB2 When the Count By Two field (bit 3) is set to 0, the address counter uses the character clock. When set to 1, the address counter uses the character clock input divided by 2. This bit is used to create either a byte or word refresh address for the display buffer.

HRS The Horizontal Retrace Select field (bit 2) selects the clock that controls the vertical timing counter. The clocking is either the horizontal retrace clock or horizontal retrace clock divided by 2. When set to 1, the horizontal retrace clock is divided by 2.

Dividing the clock effectively doubles the vertical resolution of the CRT controller. The vertical counter has a maximum resolution of 1024 scan lines because the vertical total value is 10 bits wide. If the vertical counter is clocked with the horizontal retrace divided by 2, the vertical resolution is doubled to 2048 scan lines.

SRC The Select Row Scan Counter field (bit 1) selects the source of bit 14 of the output multiplexer. When set to 0, bit 1 of the row scan counter is the source. When set to 1, bit 14 of the address counter is the source.

CMS0 The CMS 0 field (bit 0) selects the source of bit 13 of the output multiplexer. When set to 0, bit 0 of the row scan counter is the source. When set to 1, bit 13 of the address counter is the source.

The CRT controller used on the IBM Color/Graphics Adapter was capable of using 128 horizontal scan-line addresses. For VGA to obtain 640-by-200 graphics resolution, the CRT controller is programmed for 100 horizontal scan lines with two scan-line addresses per character row. Row scan address bit 0 becomes the most-significant address bit to the display buffer. Successive scan lines of the display image are displaced in 8KB of memory. This bit allows compatibility with the graphics modes of earlier adapters.

Line Compare Register

This register has an index of hex 18; its address is hex 03D5 or 03B5.

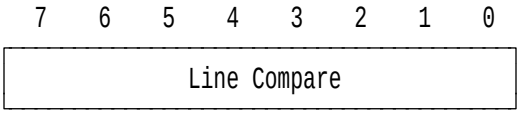


Figure 2-66. Line Compare Register, Index Hex 18

The Line Compare Register (bits 7– 0) contains the 8 low-order bits of the 10-bit compare target. When the vertical counter reaches the target value, the internal start address of the line counter is cleared. This creates a split screen in which the lower screen is immune to scrolling. Bit 8 is in the Overflow register (index hex 07), and bit 9 is in the Maximum Scan Line register (index hex 09).

Graphics Controller Registers

The Address register for the graphics controller is at address hex 03CE. The data registers are at address hex 03CF. All registers are read/write.

Register Name	Address (Hex)	Index (Hex)
Address	03CE	
Set/Reset	03CF	00
Enable Set/Reset	03CF	01
Color Compare	03CF	02
Data Rotate	03CF	03
Read Map Select	03CF	04
Graphics Mode	03CF	05
Miscellaneous	03CF	06
Color Don't Care	03CF	07
Bit Mask	03CF	08

Figure 2-67. Graphics Controller Register Overview

Address Register

The Address register is at address hex 03CE. This register is loaded with the index value that points to the desired data register within the graphics controller.

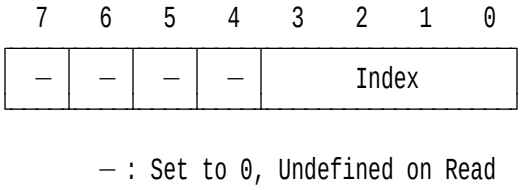


Figure 2-68. Graphics Controller Address Register, Hex 03CE

The register field is defined as follows:

Index The Index field (bits 3– 0) contains the index value that points to the data registers.

Set/Reset Register

This register has an index of hex 00; its address is hex 03CF.

7	6	5	4	3	2	1	0
–	–	–	–	SR3	SR2	SR1	SR0

```
  – : Set to 0, Undefined on Read
SR3 : Set/Reset Map 3
SR2 : Set/Reset Map 2
SR1 : Set/Reset Map 1
SR0 : Set/Reset Map 0
```

Figure 2-69. Set/Reset Register, Index Hex 00

The register fields are defined as follows:

SR3, SR2, SR1, SR0

When write mode 0 is selected, the system writes the value of each set/reset field (bits 3, 2, 1, or 0) to its respective memory map. For each write operation, the set/reset bit, if enabled, is written to all 8 bits within that map. Set/reset operation can be enabled on a map-by-map basis through the Enable Set/Reset register.

Enable Set/Reset Register

The index for this register is hex 01; its address is hex 03CF.

7	6	5	4	3	2	1	0
–	–	–	–	ESR3	ESR2	ESR1	ESR0

```
  – : Set to 0, Undefined on Read
ESR3 : Enable Set/Reset Map 3
ESR2 : Enable Set/Reset Map 2
ESR1 : Enable Set/Reset Map 1
ESR0 : Enable Set/Reset Map 0
```

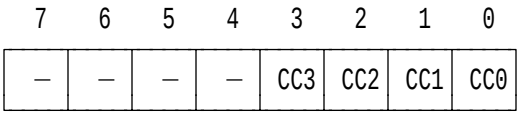
Figure 2-70. Enable Set/Reset Register, Index Hex 01

The register fields are defined as follows:

ESR3, ESR2, ESR1, ESR0
These fields (bits 3, 2, 1, and 0) enable the set/reset function used when write mode 0 is selected in the Graphics Mode register (index hex 05). When set to 1, the respective memory map receives the value specified in the Set/Reset register. When Set/Reset is not enabled for a map, that map receives the value sent by the system.

Color Compare Register

This register has an index of hex 02; its address is hex 03CF.




```
  – : Set to 0, Undefined on Read
CC3 : Color Compare Map 3
CC2 : Color Compare Map 2
CC1 : Color Compare Map 1
CC0 : Color Compare Map 0
```

Figure 2-71. Color Compare Register, Index Hex 02

The register fields are defined as follows:

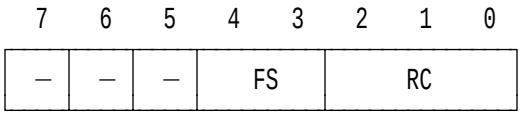
CC3, CC2, CC1, CC0

These color compare map fields (bits 3, 2, 1, and 0) make up the 4-bit color value to be compared when the read mode bit in the Graphics Mode register is set to 1. When the system does a memory read, the data returned from the memory cycle will be a 1 in each bit position where the four maps equal the Color Compare register. If the read mode bit is 0, the data is returned without comparison.

The color compare bit is the value that all bits of the corresponding map's byte are compared with. Each of the 8 bit positions in the selected byte are compared across the four maps, and a 1 is returned in each position where the bits of all four maps equal their respective color compare values.

Data Rotate Register

This register has an index of hex 03; its address is hex 03CF.



– : Set to 0, Undefined on Read
FS : Function Select
RC : Rotate Count

Figure 2-72. Data Rotate Register, Index Hex 03

The register fields are defined as follows:

FS Data written to the video buffer can be operated on logically by data already in the system latches. The Function Select field (bits 4, 3) determines whether and how this is done.

Data can be any of the choices selected by the write mode bits except system latches, which cannot be modified. If rotated data is selected also, the rotate is performed before the logical operation. The logical operations selected are shown in the following table.

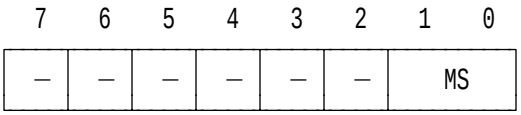
FS Field (binary)	Function
0 0	Data Unmodified
0 1	Data ANDed with Latched Data
1 0	Data ORed with Latched Data
1 1	Data XORed with Latched Data

Figure 2-73. Operation Select Bit Definitions

RC In write mode 0, the Rotate Count field (bits 2– 0) selects the number of positions the system data is rotated to the right during a system memory write operation. To write data that is not rotated in mode 0, all bits are set to 0.

Read Map Select Register

This register has an index of hex 04; its address is hex 03CF.



– : Set to 0, Undefined on Read
MS : Map Select

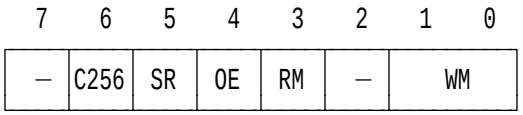
Figure 2-74. Read Map Select Register, Index Hex 04

The register field is defined as follows:

MS The Map Select field (bits 1, 0) selects the memory map for system read operations. This register has no effect on the color compare read mode. In odd/even modes, the value can be a binary 00 or 01 to select the chained maps 0, 1 and the value can be a binary 10 or 11 to select the chained maps 2, 3.

Graphics Mode Register

This register has an index of hex 05; its address is hex 03CF.




```
  – : Set to 0, Undefined on Read
C256 : 256 - Color Mode
  SR : Shift Register Mode
  OE : Odd/Even
  RM : Read Mode
  WM : Write Mode
```

Figure 2-75. Graphics Mode Register, Index Hex 05

The register fields are defined as follows:

C256 When set to 0, the 256-Color Mode field (bit 6) allows bit 5 to control the loading of the shift registers. When set to 1, this field causes the shift registers to be loaded in a manner that supports the 256-color mode.

SR When set to 1, the Shift Register Mode field (bit 5) directs the shift registers in the graphics controller to format the serial data stream with even-numbered bits from both maps on even-numbered maps, and odd-numbered bits from both maps on the odd-numbered maps. This bit is used for modes 4 and 5.

OE When set to 1, the Odd/Even field (bit 4) selects the odd/even addressing mode used by the IBM Color/Graphics Monitor Adapter. Normally, the value here follows the value of Memory Mode register bit 2 in the sequencer.

RM When the Read Mode field (bit 3) is set to 1, the system reads the results of the comparison of the four memory maps and the Color Compare register.

When set to 0, the system reads data from the memory map selected by the Read Map Select register, or by the 2 low-order bits of the memory address (this

selection depends on the chain-4 bit in the Memory Mode register of the sequencer).

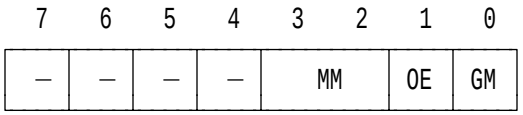
WM The Write Mode field (bits 1, 0) determines the write mode selected. The write mode selected and its operation are defined in the following figure. The logic operation specified by the function select bits is performed on system data for modes 0, 2, and 3.

WM Field (binary)	Mode Description
0 0	Each memory map is written with the system data rotated by the count in the Data Rotate register. If the set/reset function is enabled for a specific map, that map receives the 8-bit value contained in the Set/Reset register.
0 1	Each memory map is written with the contents of the system latches. These latches are loaded by a system read operation.
1 0	Memory map *n* (0 through 3) is filled with 8 bits of the value of data bit *n*.
1 1	Each memory map is written with the 8-bit value contained in the Set/Reset register for that map (the Enable Set/Reset register has no effect). Rotated system data is ANDed with the Bit Mask register to form an 8-bit value that performs the same function as the Bit Mask register in write modes 0 and 2 (see also Bit Mask register on page 2-88).

Figure 2-76. Write Mode Definitions

Miscellaneous Register

This register has an index of hex 06; its address is hex 03CF.



– : Set to 0, Undefined on Read
MM : Memory Map
OE : Odd/Even
GM : Graphics Mode

Figure 2-77. Miscellaneous Register, Index Hex 06

The register fields are defined as follows:

MM The Memory Map field (bits 3, 2) controls the mapping of the regenerative buffer into the system address space. The bit functions are defined in the following figure.

MM Field (binary)	Addressing Assignment
0 0	A0000 for 128KB
0 1	A0000 for 64KB
1 0	B0000 for 32KB
1 1	B8000 for 32KB

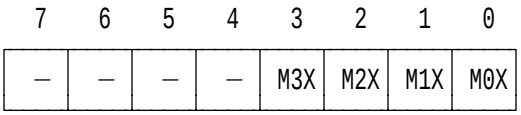
Figure 2-78. Video Memory Assignments

OE When set to 1, the Odd/Even field (bit 1) directs the system address bit, A0, to be replaced by a higher-order bit. The odd map is then selected when A0 is 1, and the even map when A0 is 0.

GM The Graphics Mode field (bit 0) controls alphanumeric mode addressing. When set to 1, this bit selects graphics modes, which also disables the character generator latches.

Color Don't Care Register

This register has an index of hex 07; its address is hex 03CF.




```
  – : Set to 0, Undefined on Read
M3X : Map 3 is Don't Care
M2X : Map 2 is Don't Care
M1X : Map 1 is Don't Care
M0X : Map 0 is Don't Care
```

Figure 2-79. Color Don't Care Register, Index Hex 07

The register fields are defined as follows:

M3X, M2X, M1X, M0X
These map don't care fields (bits 3, 2, 1, and 0) select whether a map is going to participate in the color compare cycle. When set to 1, the bits in that map are compared.

Bit Mask Register

This register has an index of hex 08; its address is hex 03CF.

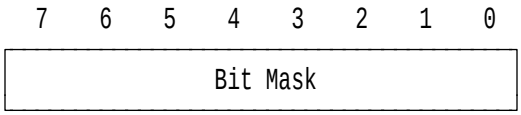


Figure 2-80. Bit Mask Register, Index Hex 08

When a bit in the Bit Mask register (bits 7– 0) is set to 1, the corresponding bit position in each map can be changed. When a bit is set to 0, the bit position in the map is masked to prevent change, provided that the location being written was the last location read by the system microprocessor.

The bit mask applies to write modes 0 and 2. To preserve bits using the bit mask, data must be latched internally by reading the location. When data is written to preserve the bits, the most current data in the latches is written in those positions. The bit mask applies to all maps simultaneously.

Attribute Controller Registers

Each register for the attribute controller has two addresses. Address hex 03C0 is the write address and hex 03C1 is the read address. The individual data registers are selected by writing their index to the Address register (hex 03C0).

Register Name	Write Address	Read Address	Index
Address	03C0	03C0	–
Internal Palette	03C0	03C1	00– 0F
Attribute Mode Control			10
Overscan Color			11
Color Plane Enable			12
Horizontal PEL Panning			13
Color Select			14

Figure 2-81. Attribute Controller Register Addresses

Address Register

This read/write register is at address hex 03C0.

The attribute controller registers do not have an input bit to control selection of the address and data registers. An internal address flip-flop controls this selection. Reading Input Status Register 1 clears the flip-flop and selects the Address register.

After the Address register has been loaded with the index, the next write operation to 03C0 loads the data register. The flip-flop toggles for each write operation to address hex 03C0. It does not toggle for Read operations to 03C0 or 03C1. (Also see “VGA Programming Considerations” on page 2-97.)

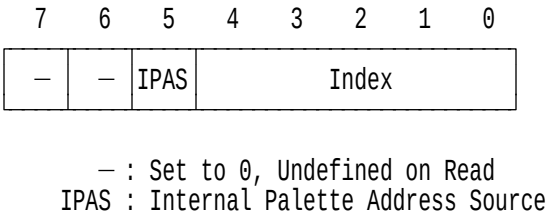


Figure 2-82. Address Register, Hex 03C0

The register fields are defined as follows:

IPAS The Internal Palette Address Source field (bit 5) is set to 0 to load color values to the registers in the internal palette. It is set to 1 for normal operation of the attribute controller.

Note: Do not access the internal palette while this bit is set to 1. While this bit is 1, the Type 1 video subsystem disables accesses to the palette; however, the Type 2 does not, and the actual color value addressed cannot be ensured.

Index The Index field (bits 4– 0) contains the index to the data registers in the attribute controller.

Internal Palette Registers 0 through F

These registers are at indexes hex 00 through 0F. Their write address is hex 03C0; their read address is hex 03C1.

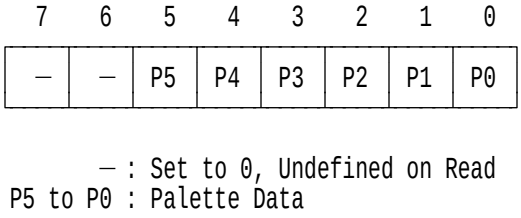


Figure 2-83. Internal Palette Registers, Index Hex 00 - 0F

The register fields are defined as follows:

P5– P0 These 6-bit registers (bits 5– 0) allow a dynamic mapping between the text attribute or graphic color input value and the display color on the CRT screen. When set to 1, this bit selects the appropriate color. The Internal Palette registers should be modified only during the vertical retrace interval to avoid problems with the displayed image. These internal palette values are sent off-chip to the video DAC, where they serve as addresses into the DAC registers. (Also see the attribute controller block diagram on page 2-10.)

Note: These registers can be accessed only when bit 5 in the Address register is set to 0. When the bit is 1, writes are “don't care” and reads return undefined data.

Attribute Mode Control Register

This read/write register is at index hex 10. Its write address is hex 03C0; its read address is hex 03C1.

7	6	5	4	3	2	1	0
PS	PW	PP	—	EB	ELG	ME	G

```
 — : Set to 0, Undefined on Read
PS : P5, P4 Select
PW : PEL Width
PP : PEL Panning Compatibility
EB : Enable Blink/—Select Background Intensity
ELG : Enable Line Graphics Character Code
ME : Mono Emulation
G : Graphics/—Alphanumeric Mode
```

Figure 2-84. Attribute Mode Control Register, Index Hex 10

The register fields are defined as follows:

PS The P5, P4 Select field (bit 7) selects the source for the P5 and P4 video bits that act as inputs to the video DAC. When set to 0, P5 and P4 are the outputs of the Internal Palette registers. When set to 1, P5 and P4 are bits 1 and 0 of the Color Select register. For more information, see “VGA Programming Considerations” on page 2-97.

PW When the PEL Width field (bit 6) is set to 1, the video data is sampled so that 8 bits are available to select a color in the 256-color mode (hex 13). This bit is set to 0 in all other modes.

PP When the PEL Panning Compatibility field (bit 5) is set to 1, a successful line-compare in the CRT controller forces the output of the PEL Panning register to 0 until a vertical synchronization occurs, at which time the output returns to its programmed value. This bit allows a selected portion of a screen to be panned.

When set to 0, line compare has no effect on the output of the PEL Panning register.

EB When the Enable Blink/– Select Background Intensity field (bit 3) is set to 0, the most-significant bit of the attribute selects the background intensity (allows 16 colors for background). When set to 1, this bit enables blinking.

ELG When the Enable Line Graphics Character Code field (bit 2) is set to 0, the ninth dot will be the same as the background. When set to 1, this bit enables the special line-graphics character codes for the monochrome emulation mode. This emulation mode forces the ninth dot of a line graphic character to be identical to the eighth dot of the character. The line-graphics character codes for the monochrome emulation mode are hex C0 through hex DF.

For character fonts that do not use these line-graphics character codes, bit 2 should be set to 0 to prevent unwanted video information from displaying on the CRT screen.

BIOS will set this bit, the correct dot clock, and other registers when the 9-dot alphanumeric mode is selected.

ME When the Mono Emulation field (bit 1) is set to 1, monochrome emulation mode is selected. When set to 0, color emulation mode is selected.

G When the Graphics/– Alphanumeric Mode field (bit 0) is set to 1, the graphics mode of operation is selected.

Overscan Color Register

This read/write register is at index hex 11. Its write address is hex 03C0; its read address is hex 03C1. This register determines the border (overscan) color.

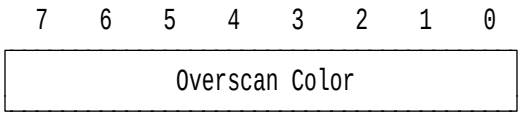


Figure 2-85. Overscan Color Register, Index Hex 11

The Overscan Color register (bits 7– 0) selects the border color used in the 80-column alphanumeric modes and in the graphics modes other than modes 4, 5, and D.

Color Plane Enable Register

This read/write register is at index hex 12. Its write address is hex 03C0; its read address is hex 03C1.

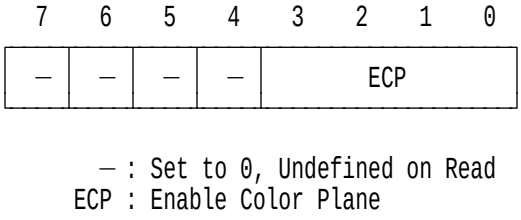


Figure 2-86. Color Plane Enable Register, Index Hex 12

The register field is defined as follows:

ECP Setting a bit in the Enable Color Plane field (bits 3– 0) to 1 enables the corresponding display-memory color plane.

Horizontal PEL Panning Register

This read/write register is at index hex 13. Its write address is hex 03C0; its read address is hex 03C1.

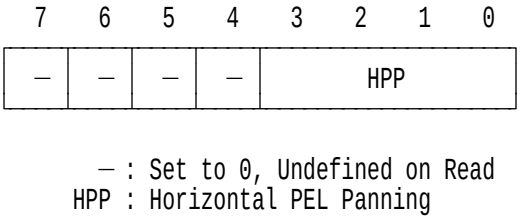


Figure 2-87. Horizontal PEL Panning Register, Index Hex 13

The register field is defined as follows:

HPP The Horizontal PEL Panning field (bits 3– 0) selects the number of PELs that the video data is shifted to the left. PEL panning is available in both alphanumeric (A/N) and graphics modes. The following figure shows the number of PELs shifted for each mode.

	Number of PELs Shifted to the Left		
Register Value	**Mode Hex 13**	**A/N Modes ***	**All Other Modes**
0	0	1	0
1	–	2	1
2	1	3	2
3	–	4	3
4	2	5	4
5	–	6	5
6	3	7	6
7	–	8	7
8	–	0	–
* Only mode 7 and the A/N modes with 400 scan lines.			

Figure 2-88. Image Shifting

Color Select Register

This read/write register is at index hex 14. Its write address is hex 03C0; its read address is hex 03C1.

7	6	5	4	3	2	1	0
–	–	–	–	SC7	SC6	SC5	SC4

```
  – : Set to 0, Undefined on Read
SC7 : S_color 7
SC6 : S_color 6
SC5 : S_color 5
SC4 : S_color 4
```

Figure 2-89. Color Select Register, Index Hex 14

The register fields are defined as follows:

SC7, SC6 In modes other than mode hex 13, the S_color 7 and S_color 6 fields (bits 3, 2) are the 2 most-significant bits of the 8-bit digital color value to the video DAC. In mode hex 13, the 8-bit attribute is the digital color value to the video DAC. These bits are used to switch rapidly between sets of colors in the video DAC. (For more information, see “VGA Programming Considerations” on page 2-97.)

SC5, SC4 The S_color 5 and S_color 4 fields (bits 1, 0) can be used in place of the P4 and P5 bits from the Internal Palette registers to form the 8-bit digital color value to the video DAC. Selecting these bits is done in the Attribute Mode Control register (index hex 10). These bits are used to switch rapidly between color sets within the video DAC.

VGA Programming Considerations

The following are some programming considerations for the VGA:

- The following rules must be followed to guarantee the critical timings necessary to ensure the proper operation of the CRT controller:
  - The value in the Horizontal Total register must be at least hex 19.
  - The minimum positive pulse width of the 'horizontal synchronization' signal must be 4 character clock units.
  - The End Horizontal Retrace register must be programmed such that the 'horizontal synchronization' signal goes to 0 at least 1 character clock time before the 'horizontal display enable' signal goes active.
  - The End Vertical Blanking register must be set to a value at least one horizontal scan line greater than the line-compare value.
- When PEL panning compatibility is enabled in the Attribute Mode Control register, a successful line compare in the CRT controller forces the output of the Horizontal PEL Panning register to 0's until a vertical synchronization occurs. When the vertical synchronization occurs, the output returns to the programmed value. This allows the portion of the screen indicated by the Line Compare register to be operated on by the Horizontal PEL Panning register.
- A write to the Character Map Select register becomes valid on the next whole character line. This prevents deformed character images when changing character generators in the middle of a character scan line.
- For mode hex 13, the attribute controller is configured so that the 8-bit attribute in video memory becomes the 8-bit address (P0 through P7) into the video DAC. The user should not modify the contents of the Internal Palette registers when using this mode.
- To achieve smooth scrolling, see "Smooth Scrolling of VGA and 132 Column Text Modes" on page 3-225.

- The following is the sequence for accessing the attribute data registers:

  1. Disable interrupts.
  2. Reset the flip-flop for the Attribute Address register.
  3. Write the index.
  4. Access the data register.
  5. Enable interrupts.

- The Color Select register in the attribute controller section allows rapid switching between color sets in the video DAC. Bit 7 of the Attribute Mode Control register controls the number of bits in the Color Select register used to address the color information in the video DAC (either 2 or 4 bits are used). By changing the value in the Color Select register, an application can switch color sets in graphics and alphanumeric modes. (Mode hex 13 does not use this feature.)

  Note: For multiple color sets, the user must load the color values.

- An application that saves the video state must store the 4 bytes of information contained in the system microprocessor latches in the graphics controller subsection. These latches are loaded with 32 bits from video memory (8 bits per map) each time the system reads from video memory. The application must:

  1. Use write mode 1 to write the values in the latches to a location in video memory that is not part of the display buffer, such as the last location in the address range.
  2. Save the values of the latches by reading them back from video memory.

     Note: If memory addressing is in the chain-4 or odd/even mode, reconfigure the memory as four sequential maps prior to performing the sequence above.

  BIOS provides support for completely saving and restoring the video state. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for more information.

- The Horizontal PEL Panning register allows programs to control the starting position of the display area on the screen. The display area can be shifted to the left up to eight PEL positions. In single-byte shift modes, to pan to more than eight PEL positions, the CRT controller start address is incremented and the Horizontal PEL Panning register is reset to 0.

  In multiple shift modes, the byte-panning bits (in the Preset Row Scan register) are used as extensions to the Horizontal PEL Panning register. This allows panning across the width of the video output. For example, in the 32-bit shift mode, the byte pan and PEL-panning bits provide panning up to 31 bits. To pan from position 31 to 32, the CRT controller start address is incremented and the panning bits, both PEL and byte, are reset to 0.

  Further panning can be accomplished by changing the start-address value in the CRT controller registers, Start Address High and Start Address Low. The sequence is:

  1. Use the Horizontal PEL Panning register to shift the maximum number of bits to the left.
  2. Increment the start address.
  3. Set the Horizontal PEL Panning register so that no bits are shifted.

     The screen is shifted one PEL to the left of the position it was in at the end of Step 1. Repeat Step 1 through Step 3 as often as necessary.

- When operating in a mode with 200 scan lines, and using a split-screen application that scrolls a second screen on top of the first screen, the Line Compare register (CRT Controller register hex 19) must contain an even value. This is a requirement of the double scanning logic in the CRT controller.
- If the value in the Cursor Start register (CRT Controller register hex 0A) is greater than that in the Cursor End register (CRT Controller register hex 0B), the cursor is not displayed.
- In 8-dot character modes, the underline attribute produces a solid line across adjacent characters. In 9-dot character modes, the underline across adjacent characters is dashed. In 9-dot modes with the line-graphics characters (C0 through DF character codes), the underline is solid.

Programming the Registers

Each of the video components has an address register and a number of data registers. The data registers have addresses common to all registers for that component. The individual registers are selected by a pointer (index) in their Address register. To write to a data register, the Address register is loaded with the index of the desired data register, then the data register is loaded by writing to the common I/O address.

The general registers do not share a common address; they each have their own I/O address.

See “Video DAC to System Interface” on page 2-104 for details on programming the video DAC.

For compatibility with the IBM Enhanced Graphics Adapter (EGA), the internal video subsystem palette is programmed the same as the EGA. Using BIOS to program the palette produces a color compatible to that produced by the EGA. Mode hex 13 (256 colors) is programmed so that the first 16 locations in the DAC produce compatible colors.

When BIOS is used to load the color palette for a color mode and a monochrome display is attached, the color palette is changed. The colors are summed to produce shades of gray that allow color applications to produce a readable screen.

Modifying the following bits must be done while the sequencer is held in a synchronous reset through its Reset register. The bits are:

- Bits 3 and 0 of the Clocking Mode register
- Bits 3 and 2 of the Miscellaneous Output register.

RAM Loadable Character Generator

The character generator is RAM loadable and can support characters up to 32 scan lines high. Three character fonts are stored in BIOS, and one is automatically loaded when an alphanumeric mode is selected. The Character Map Select register can be programmed to redefine the function of bit 3 of the attribute byte to be a character-font switch. This allows the user to select between any two character sets residing in map 2, and gives the user access to 512 characters instead of 256. Character fonts can be loaded off line, and up to eight fonts can be loaded at any one time.

The structure of the character fonts is described in the following figure. The character generator is in map 2 and must be protected using the map mask function.

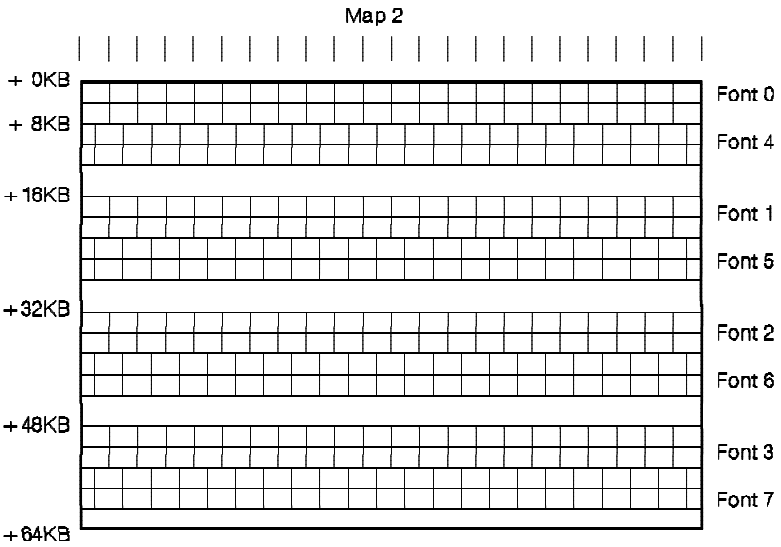


Figure 2-90. Character Table Structure

The following figure illustrates the structure of each character pattern. If the CRT controller is programmed to generate 16 row scans, then 16 bytes must be filled in for each character in the font. The example below assumes eight row scans per character.

Address	Byte Image								Data
CC * 32 + 0				X	X				18H
1			X	X	X	X			3CH
2		X	X			X	X		66H
3		X	X			X	X		66H
4		X	X	X	X	X	X		7EH
5		X	X			X	X		66H
6		X	X			X	X		66H
7		X	X			X	X		66H

*CC equals the value of the character code. For example, hex 41 equals and ASCII "A".

Figure 2-91. Character Pattern Example

Creating a Split Screen

The VGA hardware supports a split screen. The top portion of the screen is designated as screen A, and the bottom portion is designated as screen B, as in the following figure.

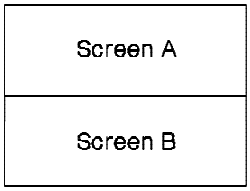


Figure 2-92. Split Screen Definition

The following figure shows the screen mapping for a system containing a 32KB alphanumeric storage buffer, such as the VGA. Information displayed on screen A is defined by the Start Address High and Low registers of the CRT controller. Information displayed on screen B always begins at video address hex 0000.

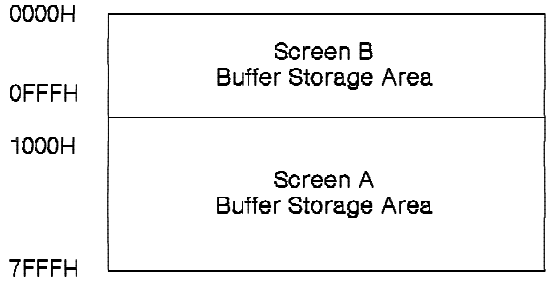


Figure 2-93. Screen Mapping within the Display Buffer Address Space

The Line Compare register of the CRT controller performs the split screen function. The CRT controller has an internal horizontal scan line counter and logic that compares the counter value to the value in the Line Compare register and clears the memory address generator when a comparison occurs. The linear address generator then sequentially addresses the display buffer starting at location 0. Each subsequent row address is determined by the 16-bit addition of the start-of-line latch and the Offset register.

Screen B can be smoothly scrolled onto the display by updating the Line Compare register in synchronization with the 'vertical retrace' signal. Screen B information is not affected by scrolling operations that use the Start Address registers to scroll through screen A information.

When PEL-panning compatibility is enabled (Attribute Mode Control register), a successful line comparison forces the output of the Horizontal PEL Panning register to 0's until vertical synchronization occurs. This feature allows the information on screen B to remain unaffected by PEL-panning operations on screen A.

Video Digital-to-Analog Converter

The video digital-to-analog converter (DAC) integrates the function of a color palette with three internal DACs for driving an analog display.

The DAC has 256 registers containing 18 bits each to allow the display of up to 256 colors from a possible 256k colors. Each output signal is driven by a 6-bit DAC.

Register Name	Read/ Write	Address (in Hex)
Palette Address (Write Mode)	R/W	03C8
Palette Address (Read Mode)	W	03C7
DAC State	R	03C7
Palette Data	R/W	03C9
PEL Mask	R	03C6

Figure 2-94. Video DAC Register

Device Operation

The palette address (P7 through P0) and the blanking input are sampled on the rising edge of the PEL clock. After three more PEL clock cycles, the video reflects the state of these inputs.

During normal operation, the palette address is used as a pointer to one of the 256 data registers in the palette. The value in each data register is converted to an analog signal for each of the three outputs (red, green, blue). The blanking input is used to force the video output to 0 volts. The blanking operation is independent of the palette operation.

Each data register is 18 bits wide: 6 bits each for red, green, and blue. The data registers are accessible through the system interface.

Video DAC to System Interface

The Palette Address register holds an 8-bit value that is used to address a location within the video DAC. The Palette Address register responds to two addresses; the address depends on the type of palette access, read or write. Once the address is loaded, successive accesses to the data register automatically increment the address register.

For palette write operations, the address for the Palette Address register is hex 03C8. A write cycle consists of writing three successive bytes to the Data register at address hex 03C9. The 6 least-significant bits of each byte are concatenated to form the 18-bit palette data. The order is red value first, then green, then blue.

For palette read operations, the address for the Palette Address register is hex 03C7 (in the read mode, the Palette Address register is write only). A read cycle consists of reading three successive bytes from the Data register at address hex 03C9. The 6 least-significant bits of each byte contain the corresponding color value. The order is red value first, then green, then blue.

If the Palette Address register is written to during a read or write cycle, a new cycle is initialized and the unfinished cycle is terminated. The effects of writing to the Data register during a read cycle or reading from the Data register during a write cycle are undefined and can change the palette contents.

The DAC State register is a read-only register at address hex 03C7. Bits 1 and 0 return the last active operation to the DAC. If the last operation was a read operation, both bits are set to 1. If the last operation was a write, both bits are set to 0.

Reading the Read Palette Address register at hex 03C8 or the DAC State register at hex 03C7 does not interfere with read or write cycles.

Programming Considerations

- As explained in “Video DAC to System Interface” on page 2-104, the effects of writing to the Data register during a read cycle or reading from the Data register during a write cycle are undefined and can change the palette contents. Therefore, the following sequence must be followed to ensure the integrity of the color palette during accesses to it:

  1. Disable interrupts.
  2. Write the address to PEL Address register.
  3. Write or read three bytes of data.
  4. Go to Step 2, repeat for the desired number of locations.
  5. Enable interrupts.

  Note: All accesses to the DAC registers are byte-wide I/O operations.

- To prevent “snow” on the screen, an application reading data from or writing data to the DAC registers should ensure that the blank input to the DAC is asserted. This can be accomplished either by restricting data transfers to retrace intervals (use Input Status Register 1 to determine when retrace is occurring) or by using the screen off bit located in the Clocking Mode register in the sequencer.

  Note: BIOS provides read and write interfaces to the video DAC.

- Do not write to the PEL Mask register (hex 03C6). Palette information can be changed as a result. This register is correctly initialized to hex FF during a mode set.

VGA Video Extensions

The video extensions provide a means of transferring video information between the base video subsystem and an auxiliary video adapter.

The video extensions consist of:

- The auxiliary video extension
- The base video extension
- The auxiliary video signals.

The base video is provided by the video subsystem integrated onto the system board, or, when not provided on the system board, by a suitable video adapter. Such an adapter can provide a Micro Channel connector with the base video extension. Video adapters supporting the base video extension must provide the VGA function as the default. For detailed connector dimensions, see Micro Channel Adapter Design in *Personal System 2 Hardware Interface Technical Reference - Architectures*.

The buffers for the base video can be turned off to allow video output from the auxiliary video to be sent through the base video DAC to the display. The video extension can be driven in only one direction at a time.

Note: The video extension supports only the VGA function (see Figure 2-97 on page 2-111).

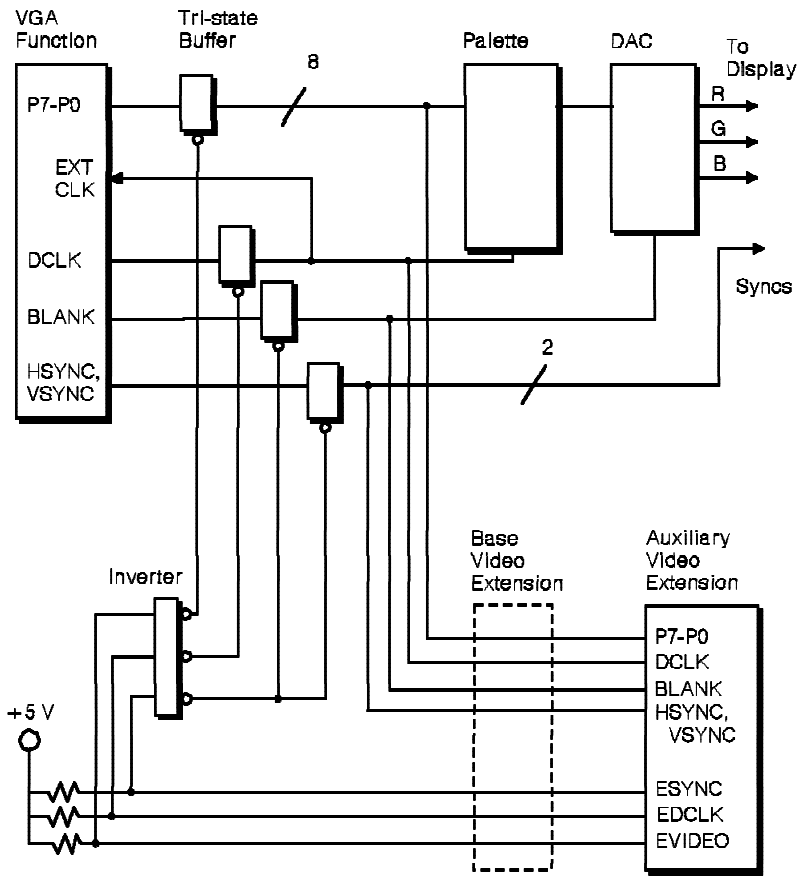


Figure 2-95. Auxiliary Video Connector Interface

Auxiliary Video Extension

This extension provides a video adapter with the ability to access the resources of the base video subsystem.

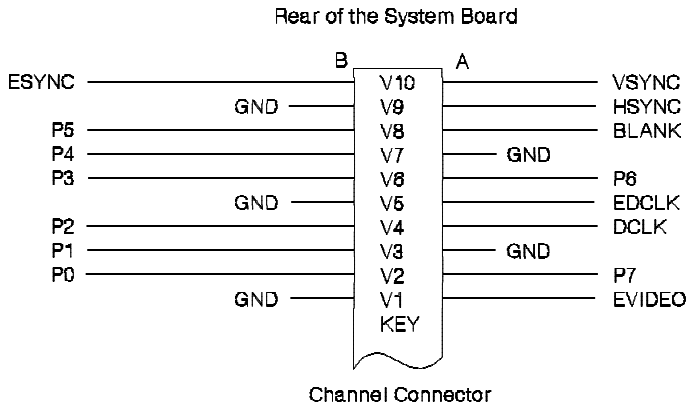


Figure 2-96. Video Extension

The auxiliary video extension is an optional part of the 16- or 32-bit Micro Channel connector.

Note: For more information on the auxiliary and base video connectors and extensions, see Micro Channel Architectures in *Personal System 2 Hardware Interface Technical Reference - Architectures*.

Base Video Extension

This extension is for adapters that provide the base video subsystem. Only systems without a base video subsystem on the system board have a connector with this extension. The base video extension signals and auxiliary video extension signals are identical.

Video adapters supporting the base video extension must provide the VGA function as the default.

The base video extension is an optional part of the 16- or 32-bit Micro Channel connector and is positioned at the end of the matched memory extension.

Video Extension Signal Descriptions

The following are signal descriptions for the auxiliary and base video extensions of the channel connector.

VSYNC: Vertical Synchronization: This signal is the vertical synchronization signal to the display. Also see the ESYNC description.

HSYNC: Horizontal Synchronization: This signal is the horizontal synchronization signal to the display. Also see the ESYNC description.

BLANK: Blanking Signal: This signal is connected to the BLANK input of the video DAC. When active (0 V dc), this signal tells the DAC to drive its analog color outputs to 0 V dc. Also see the ESYNC description.

P7– P0: Palette Bits: These eight signals contain video information and comprise the PEL address inputs to the video DAC. See also the EVIDEO description.

DCLK: Dot Clock: This signal is the PEL clock used by the DAC to latch the digital video signals, P7 through P0. The signals are latched into the DAC on the rising edge of DCLK.

This signal is driven through the EXTCLK input to the VGA when DCLK is driven by the adapter. If an adapter is providing the clock, it must also provide the video data to the DAC. Also see the EDCLK description.

ESYNC: External Synchronization: This signal is the output-enable signal for the buffer that drives BLANK, VSYNC, and HSYNC. ESYNC is tied to + 5 V dc through a pull-up resistor. When ESYNC is high, the VGA drives BLANK, VSYNC, and HSYNC. When ESYNC is pulled low, the adapter drives BLANK, VSYNC, and HSYNC.

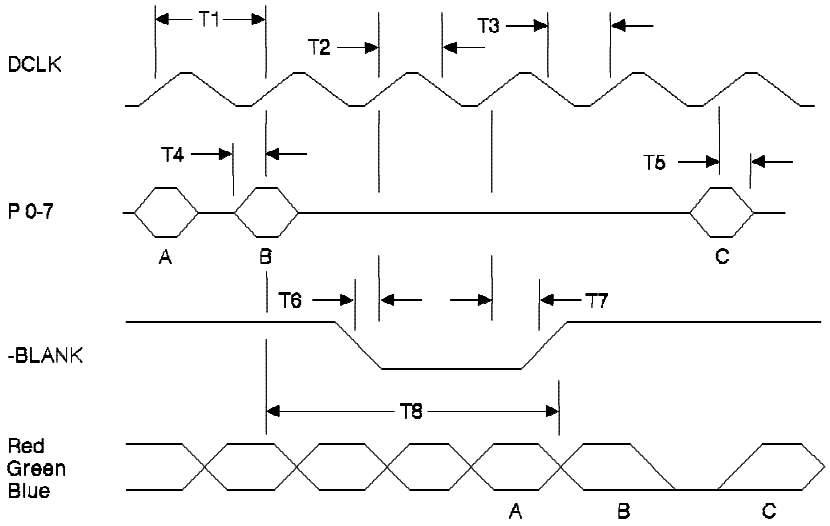
EVIDEO: External Video: This signal is the output-enable signal for the buffer that drives P7 through P0. EVIDEO is tied to + 5 V dc through a pull-up resistor. When EVIDEO is high, the VGA drives P7 through P0. When it is pulled low, the adapter drives P7 through P0.

EDCLK: External Dot Clock: This signal is the output-enable signal for the buffer that drives DCLK. EDCLK is tied to + 5 V dc through a pull-up resistor.

When EDCLK is high, the VGA is the source of DCLK to the DAC and the adapter. The Miscellaneous Output register should not select clock source 2 (010 binary) when EDCLK is high.

When EDCLK is pulled low, the adapter drives DCLK. If the adapter is driving the clock, it must also provide the video data to the DAC, and the Miscellaneous Output register must select clock source 2 (010 binary).

Video Extension Signal Timing



Symbol	Description	Minimum (ns)	Maximum (ns)
T1	PEL Clock Period	28	10,000
T2	Clock Pulse Width High	7	10,000
T3	Clock Pulse Width Low	9	10,000
T4	PEL Set-Up Time	4	–
T5	PEL Hold Time	4	–
T6	Blank Set-Up Time	4	–
T7	Blank Hold Time	4	–
T8	Analog Output Delay	3(T1) + 5	3(T1) + 30

Figure 2-97. Video Extension Signal Timing (DAC Signals)

| **Note:** Some Video Subsystems drive VGA video at video rates
| higher than those specified here. This is done to achieve higher
| screen refresh rates and better front of Screen quality (less
| flicker).

| When this is the case, the Video Extension will be disabled and will
| not available for use.