The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

TMS 5220
VOICE SYNTHESIS PROCESSOR
DATA MANUAL

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1. INTRODUCTION

1.1 SCOPE

This manual describes in detail the functional characteristics of a linear predictive coding (LPC) speech synthesis device, the TMS 5220. In addition to this document, the user may wish to refer to the TMS 6100 128K bit ROM electrical specification.

1.2 KEY FEATURES

- High-quality voice communication from a microcomputer system
- Low-data-rate LPC encoding
- Low-cost P-channel MOS technology
- +5 V and −5 V supplies only
- Interrupt-based service requests
- TTL compatible

1.3 DEVICE OPERATION

The TMS 5220 Voice Synthesis Processor (VSP) enables verbal communication with a microcomputer based system. The VSP is fabricated using P-channel MOS technology and is TTL compatible.

Speech data that has been compressed using pitch-excited linear predictive coding (LPC), is supplied to the VSP either by the CPU or by direct serial access of a Voice Synthesis Memory (VSM). The VSP decodes this data to construct a time-varying digital filter model of the vocal tract. This model is excited with a digital representation of either glottal air impulses (voiced sounds) or the rush of air (unvoiced sounds). The output of this model is passed through an eight-bit digital-to-analog converter to produce a synthetic speech waveform.

The VSP has been designed to minimize the data rate required to produce synthetic speech and to simplify the interface with the host CPU. The CPU may service the device either in a polled fashion, by monitoring device status, or by responding to interrupt service requests generated by the VSP. A simplified block diagram of the VSP is shown in Figure 1.

2. SYSTEM CLOCK

This manual describes all VSP timing based on an 8-kHz sample rate (limiting the output frequency to 4 kHz) and a 40-Hz frame rate (the rate at which new speech data is fetched and processed). This requires the internal RC oscillator in the VSP to run at 640 kHz. The user has the mask-programmable option of balancing the internal oscillator with a resistor (completing the RC network).

The 640-kHz clock is divided by four to produce two major phases, PHI-1 and PHI-2, with corresponding precharge clocks, PHI-3 and PHI-4 (see Appendix A). All control and timing operations within the VSP occur on one of the two 6.25-microsecond major phases. Twenty of these 6.25-microsecond bit times comprise each sample period (8-kHz sample rate). Twenty-five of these 125-microsecond sample periods make up one 3.25-millisecond interpolation interval, eight of which (IC0-IC7) make up the 25-millisecond frame period. During IC0, new speech data is transferred to the Synthesizer, at a 40-Hz frame rate.

3. CPU INTERFACE

The CPU interface consists of an eight-bit bidirectional data bus (D0-D7), separate selects for read operations and write operations ($\overline{RS}$ & $\overline{WS}$), a ready line for synchronization ($\overline{READY}$) and an interrupt line ($\overline{INT}$) to indicate a status change on the VSP that requires CPU attention.

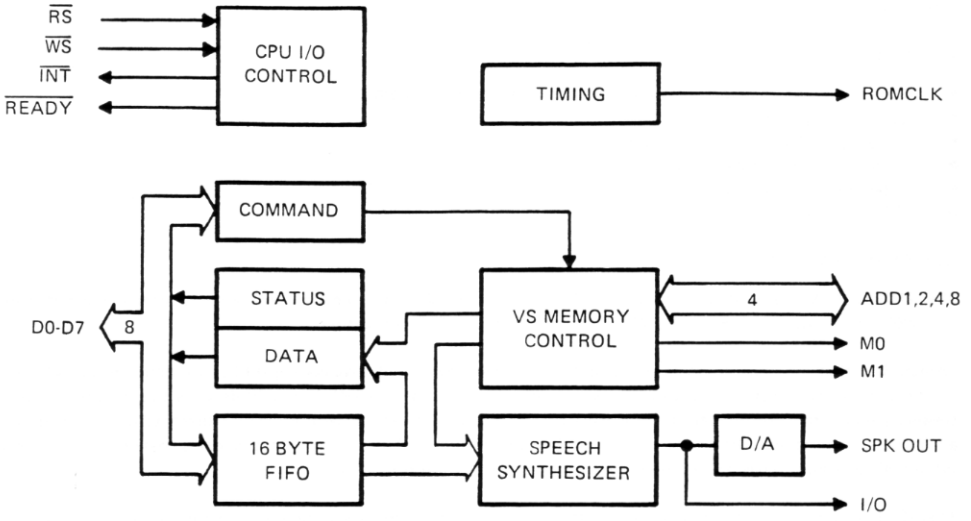


FIGURE 1 – VOICE SYNTHESIS PROCESSOR BLOCK DIAGRAM

3.1 $\overline{RS}$ AND $\overline{WS}$

VSP activity on the memory data bus is controlled by the select lines as shown below.

TABLE 1 – $\overline{RS}$ AND $\overline{WS}$ FUNCTION

$\overline{RS}$	$\overline{WS}$	BUFFER CONDITION
H	H	High impedance state
H	L	Input to VSP. Some other device must be driving the bus (typically the CPU)
L	H	Output from VSP. No other device should be driving the bus at this time.
L	L	Illegal condition. Results not predictable.

It is important to note that no device can successfully complete a Read cycle (from the VSP) while $\overline{WS}$ is active (low) nor can a successful Write cycle (to the VSP) be carried out while $\overline{RS}$ is active (low). Device behavior cannot be predicted if both $\overline{WS}$ and $\overline{RS}$ go active simultaneously. System logic should be designed to prevent this condition from occurring.

3.2 $\overline{\text{READY}}$

The VSP is a "Slow Memory"[1] device requiring wait states from the CPU to successfully complete a memory cycle. The effect of inserting wait states into memory access cycles is to extend the minimum allowable access time by one clock period for each wait state. The VSP controls the number of wait states executed by the CPU with the $\overline{\text{READY}}$ signal. The logic timing for typical read and write cycles to the VSP is shown in Figure 2.

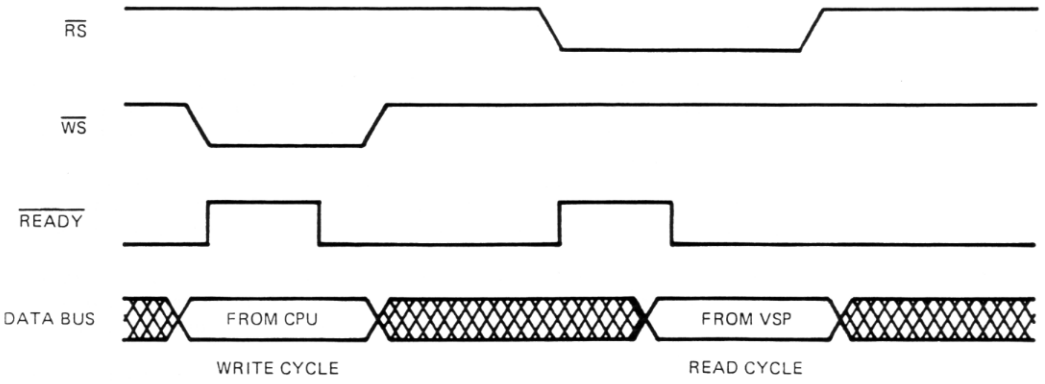


FIGURE 2 – READ AND WRITE CYCLES TO THE VSP

The $\overline{\text{READY}}$ line on the VSP goes high 100 ns after $\overline{\text{RS}}$ or $\overline{\text{WS}}$ goes active (low) to let the CPU know that the data transfer cycle cannot yet be completed. When the VSP has established stable data on the data bus (in the case of $\overline{\text{RS}}$) or has completed latching data in from the data bus (in the case of $\overline{\text{WS}}$), the $\overline{\text{READY}}$ line will go low indicating that the CPU may complete the data transfer cycle.

3.3 INTERRUPTS

The interrupt line ($\overline{\text{INT}}$) indicates changes in the status of the VSP that may require CPU attention. $\overline{\text{INT}}$ goes active (low) when any of the following occur:

- Talk Status (TS) makes a one-to-zero transition indicating the end of speech processing.
- Buffer Low (BL) makes a zero-to-one transition indicating that more phrase data needs to be supplied to the FIFO for Speak External Command.
- Buffer Empty (BE) makes a zero-to-one transition indicating that the CPU failed to supply data fast enough for a Speak External Command.[2]

$\overline{\text{INT}}$ goes inactive (high) when the Status Register is read, or if the Reset instruction is executed.

4. VOICE SYNTHESIS MEMORY (VSM) – (TMS 6100)

In addition to receiving speech data from the CPU, the VSP may directly access up to 16 TMS 6100's (128K-bit serial ROM) with no external hardware required. This is accomplished with a four-bit parallel bus (ADD8,4,2,1), (ADD8 is multiplexed as the Data Out line out of the TMS 6100 as well as the most-significant bit of the 4-bit address bus into the TMS 6100), two control lines (M0, M1), and a synchronizing clock (ROMCLK).

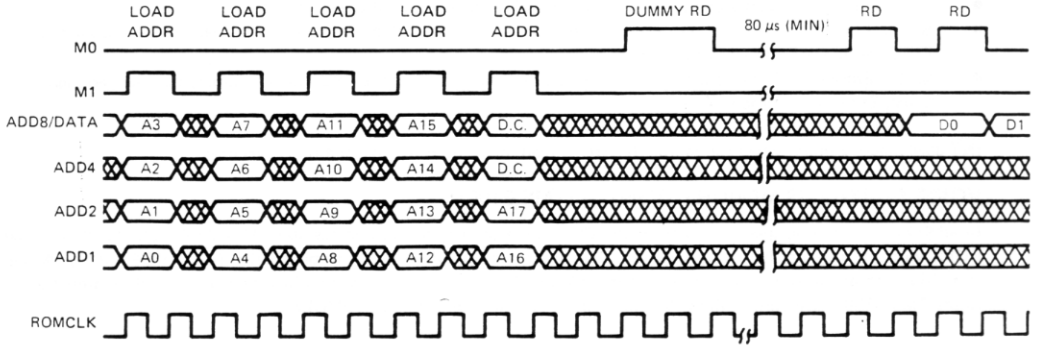
[1]Slow Memory devices are those devices that cannot properly respond to system memory cycles within the minimum access time as determined by the CPU clock rate.

[2]An interrupt will be generated at the initiation of a Speak External Instruction if BE was previously low.

The TMS 6100 is a mask programmable 128K-bit-Read-Only Memory internally organized as 16K words of eight bits; externally it appears as 128K X 1. Once the 20-bit address (14 bits to select a byte within the device, four chip select bits, two bits ignored) is loaded through ADD1, ADD2, ADD4, and ADD8 in five Load Address sequences, data is read out bit-wise by toggling a control pin (M0). The ROM contains an on-chip address counter that is incremented every eight bits (eight toggles of M0). The four internal chip select bits are a mask programmable option, and allow parallel connection of up to 16 ROMs (about 30 minutes of speech) without the need of external select circuitry.

M0	M1	FUNCTION
L	L	Idle – The passive NOP state of TMS 6100
L	H	Load Address – The four bits of data on ADD8,4,2,1 are loaded to the internal address register at the location indicated by the TMS 6100 Load Pointer. After each Load Address function, the Load Pointer is advanced to the left by four bit positions to allow the next most-significant nibble of the address to be properly loaded. The first read function[3], following a Load Address function, resets the Load Pointer to the LS bit and initiates a ROM access to fetch the address data byte. This is the only function of this "Dummy Read". No data is transferred out of VSM until the second read function following a Load Address.
H	L	Read – When the addressed data byte has been fetched and stored in the VSM Data Register, it is ready to be serially transferred out starting with the MSB. Each successive read function causes the next least-significant bit to be driven on the Data Out line of the VSM that is currently selected. The next data byte is being fetched at the same time the serial transfer is taking place so that when the last bit of the current byte is transferred, the VSM Data Register can be reloaded without delay. When the Read function immediately follows a Load Address function, it is treated as a "Dummy Read". No data is transferred, but the Load Pointer is reset and ROM access is initiated.
H	H	Read and Branch – Starting at the current address, two bytes are fetched from the ROM to form a 16-bit word. The 14 low-order bits of this word replace the 14 low-order bits of the Address Register. The Load Pointer is then reset and a ROM access initiated to fetch the byte at this new address.*

Figure 3 shows a typical sequence of loading the Address Register and reading two data bits back. For more critical timing constraints, consult the TMS 6100 Electrical Specification.



NOTE: A0 is the LSB in 6100 address.

FIGURE 3 – TMS 6100 FUNCTION TIMING

[3]A minimum of two Load Address instructions are required to change the VSM address.

*Read and Branch will not work with multiple VSM systems. Bus contention will occur.

5. I/O STRUCTURE

The VSP has two input holding registers, a Command Register and a 128-bit FIFO Buffer, and two output holding registers, the Data Register and the Status Register. On a Write cycle from the CPU, when $\overline{WS}$ becomes active (low), the control logic of the VSP routes data from the Memory Data Bus to either the FIFO Buffer (if a Speak External command is executing) or the Command Register (all other cases). Once this data has been latched in, the VSP signals completion of the data transfer to the CPU by lowering the $\overline{READY}$ Line to its active (low) condition. Similarly, on a Read cycle, when $\overline{RS}$ goes active (low), the VSP puts either the contents of the Data Register on the bus (if the preceding command was a Read Byte command) or the contents of the Status Register (all other cases).

5.1 COMMAND REGISTER

The Command Register receives command data from the Memory Data Bus and holds it for the Controller to interpret and execute. The VSP behaves as an attached processor to the host CPU and performs its synthesis tasks when appropriate commands are sent by the host CPU. For details on available commands and format, see Section 6.

5.2 FIFO BUFFER

The 128-bit FIFO Buffer is organized as a 16-byte parallel-in, serial-out buffer. This buffer is used to hold speech data passed from the CPU to be processed by a Speak External command in the VSP. As required by the synthesis section, data is shifted out serially starting with the LSB from the "First-In" byte. When this byte has been exhausted, the stack ripples down one byte and begins shifting out bits from the new "First-In" byte. A Stack Pointer keeps track of the location of the "Last-In" byte and data from the CPU is always loaded just above this location. When the stack becomes less than half full (i.e., eight byte locations are void of data), the buffer-low status condition (BL) becomes true. This signals the CPU that more data should be provided to the VSP. Under worst-case conditions, the buffer will be completely empty in one more frame period (25 milliseconds), and invalid data will be processed as external speech data. As a Fail-Safe measure, if the buffer does reach such a condition, the buffer empty status (BE) becomes true and the Talk Status Latch is reset causing speech to terminate immediately. To resume speech with data provided by the CPU, another Speak External command must be issued.

5.3 DATA REGISTER

The eight-bit Data Register is organized as a serial-in parallel-out Holding Register. This register is used by the VSP to formulate a byte of data from serial data fetched from the VSM during the execution of a Read Byte command. Data is loaded to the Data Register so that the last bit loaded is in the least-significant-bit location (D7). When the Data Register has been loaded and $\overline{RS}$ goes active (low), this byte is transferred to the Memory Data Bus (D0 = MSB). The $\overline{READY}$ Line goes low when the data is stable.

5.4 STATUS REGISTER

The three bits of the Status Register provide up-to-date information to the CPU on the state of the VSP. The Status Register may be read at any time except immediately after passing a Read Byte command to the VSP. When $\overline{RS}$ goes active (low) the VSP routes the status data to the Memory Data Bus (D0 = TS; D1 = BL; D2 = BE) and lowers the Ready Line when the data is stable.

TS – Talk Status is active (high) when the VSP is processing speech data. Talk Status goes active at the initiation of a Speak command or after nine bytes of data are loaded into the FIFO following a Speak External command. It goes inactive (low) when the stop code (Energy = 1111) is processed, or immediately by a buffer empty condition or a reset command. Audio output is interpolating to zero during this frame and is terminated on the next frame boundary.

BL – Buffer Low is active (high) when the FIFO Buffer is more than half empty. Buffer Low is set when the "Last-In" byte is shifted down past the half-full boundary (becomes the eighth data byte) of the stack. Buffer Low is cleared when data is loaded to the stack so that the "Last-In" byte lies above the half-full boundary and becomes the ninth data byte of the stack.

BE – Buffer Empty is active (high) when the FIFO Buffer has run out of data while executing a Speak External command. Buffer Empty is set when the last bit of the "Last-In" byte is shifted out to the Synthesis Section. This causes Talk Status to be cleared. Speech is terminated at some abnormal point and the Speak External command execution is terminated. Data from the Memory Data Bus is once again routed to the Command Register.

6. DESCRIPTION OF COMMANDS

The VSP operates under the control of the CPU to a minimal degree. The CPU passes commands to the VSP which initiates an activity but the CPU is not involved in carrying out that activity. Commands available for use by the CPU and the formats of these commands are shown below:

TABLE 2 – VSP COMMANDS AND COMMAND FORMAT

DATA BUS COMMAND CODE (D0-D7)*	OPERATION
X000XXXX	Nop
X001XXXX	Read Byte
X010XXXX	Nop
X110XXXX	Speak External
X011XXXX	Read and Branch
X100AAAA*	Load Address
X101XXXX	Speak
X111XXXX	Reset

*A = Address
X = Don't care

When $\overline{WS}$ becomes active (low), assuming a Speak External command is not presently executing, the data on the memory data bus is latched into the command register. Once the transfer has been completed, the VSP activates (low level) the $\overline{READY}$ line to release the CPU and begins interpreting and executing the command. Command execution for each instruction is described below.

If the user tries to pass a command to the VSP while another command is executing, the new command will not be accepted until the previous command is completed. The VSP keeps the CPU executing wait states until it is ready to accept a new command. Appendix C lists execution times for each command. The VSP uses the $\overline{READY}$ flag to tell the CPU to execute wait states until the present command has been fully executed.

6.1 READ BYTE

The Read Byte command allows the CPU to access data stored in the TMS 6100 VSM. Read Byte causes the next eight bits to be read from the VSM (ignoring byte boundaries). These bits are packed into the data register so that the last bit read from VSM is in the least-significant-bit position (D7). When $\overline{RS}$ goes active (low), and before initiation of a new instruction, this data byte is placed on D0-D7.

This eight-bit transfer from the VSM requires 80 microseconds. If $\overline{RS}$ should become active before the data register is completely loaded and ready to be transferred, the VSP keeps the CPU executing wait states (by not lowering the $\overline{READY}$ line) until the data transfer from VSM is complete and the Data Byte is stable on the Memory Data Bus. At this time the $\overline{READY}$ line is activated and the CPU may accept the Data Byte to complete the memory cycle.

6.2 READ AND BRANCH

The Read and Branch command causes the VSP to initiate a Read and Branch function on the VSM (see VSM description). The VSP is not able to access the VSM for 240 microseconds after executing this command.

6.3 LOAD ADDRESS

The Load Address command allows the CPU to alter the Address Register of the TMS 6100 to point to new speech data. Load Address causes the VSP to load the four address bits from the VSP Address Register to one nibble of the VSM Address Register by initiating a VSM Load Address function (see VSM description). If the next command following is a Read Byte, Speak, or Reset command, a dummy Read function is passed to the VSM before that next command is executed. Bit D7 is loaded into ADD1 which is the LSB of the VSM address. Bit D4 is loaded into ADD8.

6.4 SPEAK

The Speak command allows speech to be generated from phrase data stored in the VSM. The Speak command generates an internal signal that immediately causes Talk Status to be set and initiates speech synthesis calculations using the next available data from the VSM. Audio output begins on the following frame boundary. The VSP continues to fetch data from the VSM and generates speech output until a stop code (Energy = 1111) is received and recognized. At such time the audio output begins to interpolate down to the zero energy level. On the next frame boundary, speech has ended and the Talk Status is cleared. This completes execution of the Speak command. Execution of the Speak command may also be halted by the execution of Reset command. This causes audio output to halt immediately (without waiting for a frame boundary) and Talk Status to be cleared.

6.5 SPEAK EXTERNAL

The Speak External command allows the CPU to supply speech data to the VSP from some memory other than the VSM. Upon receipt of a Speak External command, the VSP purges the FIFO buffer (BL and BE becomes active [high]) and directs data written into the VSP to this buffer. The VSP idles waiting for the CPU to fill the buffer before speech begins. When the buffer low status becomes false (by the CPU loading a minimum of nine bytes to the FIFO), Talk Status is set and speech synthesis calculations begin using data from the FIFO. Data continues to be taken from the FIFO until a stop code is encountered or the buffer empty abnormal termination occurs. While the Speak External command is executing, all data written to the VSP is routed to the FIFO buffer. A Reset command is not recognized as a command.

6.6 RESET

The Reset command allows the CPU to halt the Speak command and to put the VSP into a known state. Reset clears Talk Status, halting speech activity immediately. The 128-bit FIFO Buffer is purged (BL and BE become active [high]) and the I/O paths are set to their default condition (Memory Data Bus → Command Register; Status Register → Memory Data Bus). A Load Address function is given to the VSM (using dummy address data) followed by a "Dummy Read" function.

The Reset command cannot halt the Speak External command. Flow diagrams for each instruction are given in Appendix B. System timing diagrams may be found in Appendix C.

7. POWER-UP CLEAR

The VSP contains internal circuitry to ensure a clear condition 95 percent of the time upon power-up, provided the ($V_{SS} - V_{DD}$) rise time to +10 volts is less than 2 milliseconds. If more than one power supply is used, the voltages need to be supplied to the VSP simultaneously. The Power-Up Clear sequence is finished 15 milliseconds after ($V_{SS} - V_{DD}$) reaches +10 volts. The events caused by the Power-Up Clear are similar to the Reset command and are noted below:

- Talk Status is cleared and any speech activity is halted.
- The T State Counter is reset.
- The FIFO is purged (BL & BE go active [high]) possibly causing the INT line to become active (low).
- I/O multiplexers are set to allow data to be written to the Command Register, and Data Read from the Status Register.
- The TMS 6100 is put into a known state by issuing a Load Address (using arbitrary address data) followed by a "Dummy Read".

If the user requires higher reliability in securing initialization, he should execute his own initialization sequence. A 100-percent assurance can be given that the VSP is in a clear state by writing nine bytes of all "ones" to the VSP followed by a Reset command, provided that ($V_{SS} - V_{DD}$) rise time to +10 volts is less than 2 milliseconds.

8. SPEECH SYNTHESIS

As previously mentioned, speech data fed to the VSP is encoded using pitched-excited LPC. The process of recovering this data is described briefly here and in more detail in the following sections. (This information is intended solely for the reader's information. Proper application of the VSP does not depend on a thorough understanding of this process). A simplified block diagram of the speech synthesis element of the VSP is shown in Figure 4.

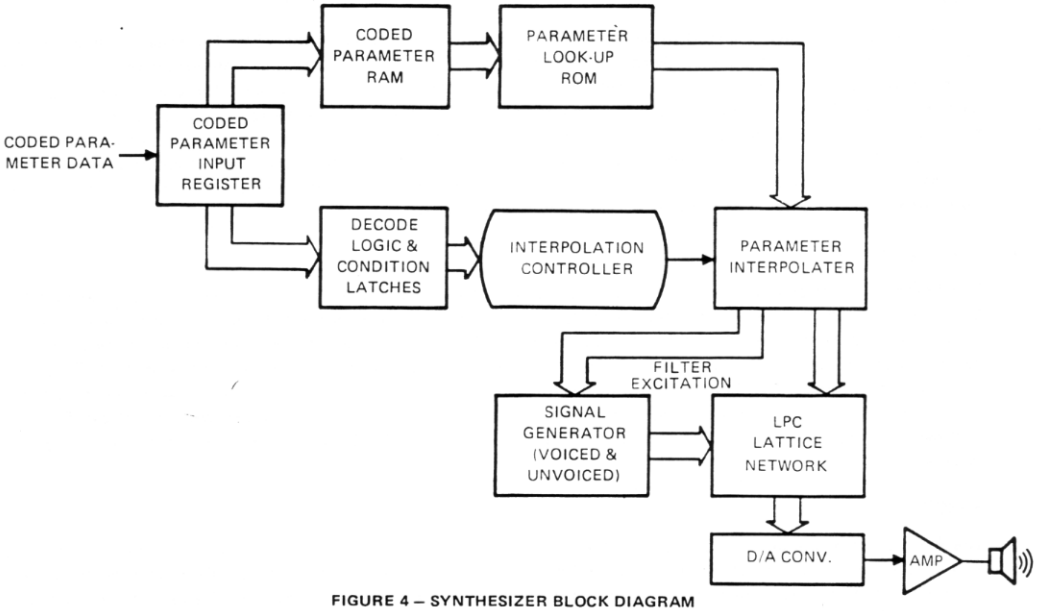


FIGURE 4 – SYNTHESIZER BLOCK DIAGRAM

Coded speech parameter data is fed serially from either the VSM or the FIFO buffer to the Parameter Input Register. Here the Controller unpacks the data and performs various tests (i.e., is the repeat bit set, is pitch zero, is energy zero). Once unpacked the coded parameter data is stored in RAM to be used as the index value to select the appropriate value from the Parameter Look-Up ROM. The outputs of the Parameter Look-Up ROM are the target values for the interpolation logic to reach in this frame period. During each of the eight interpolation periods the interpolation logic sends new pitch and energy parameters to the signal generator which produces the filter excitation sequence, and new K-parameter values to the LPC lattice network. So, at the end of each sample period there is a new value of digitized synthetic speech available to the D/A converter.

8.1 CODED SPEECH PARAMETERS

The 12 synthesis parameters (pitch, energy and reflection coefficients K1-K10), are stored in the VSM in coded form. Each parameter occupies between 3-6 bits. These coded values select a 10-bit actual parameter from the parameter Look-Up ROM. Depending on the influence of each parameter on speech quality, between 8 and 64 possible values are stored in the Look-Up ROM for decoding and use in synthesis calculations. Table 3 summarizes parameter coding for the TMS 5220.

TABLE 3 – PARAMETER CODING

PARAMETER	LEVELS	CODE BITS
ENERGY	15*	4
PITCH	64	6
K1	32	5
K2	32	5
K3	16	4
K4	16	4
K5	16	4
K6	16	4
K7	16	4
K8	8	3
K9	8	3
K10	8	3
12	247	49 + REPEAT = 50 BITS

*Energy = 1111 is the stop code.

A full set of coded parameters for each frame would require a data rate of 40 Hz X 50 bits = 2000 bits per second. Three special cases, in which a full frame is not necessary, allow the data rate to be considerably reduced:

(1) Since the vocal tract changes shape relatively slowly, it is often possible to repeat previous reflection coefficient data. To facilitate the repeat feature, a control bit has been added to each frame (an additional bit following energy). If the repeat bit is 1, only energy and pitch data are accessed from the VSM and the previous K1-K10 values are retained.

(2) Unvoiced speech requires fewer filter reflection coefficients. When Pitch = 000000, only K1-K4 are fetched from the VSM and stored in the Parameter RAM. K5-K10 are zeroed.

(3) When Energy = 0000 no other data is required. Energy = 0000 during interword or intersyllable pauses. The combination of these three cases has reduced average data rate for male speech to approximately 1200 bits per second.

Figure 5 shows the four possibilities of frame data string lengths.

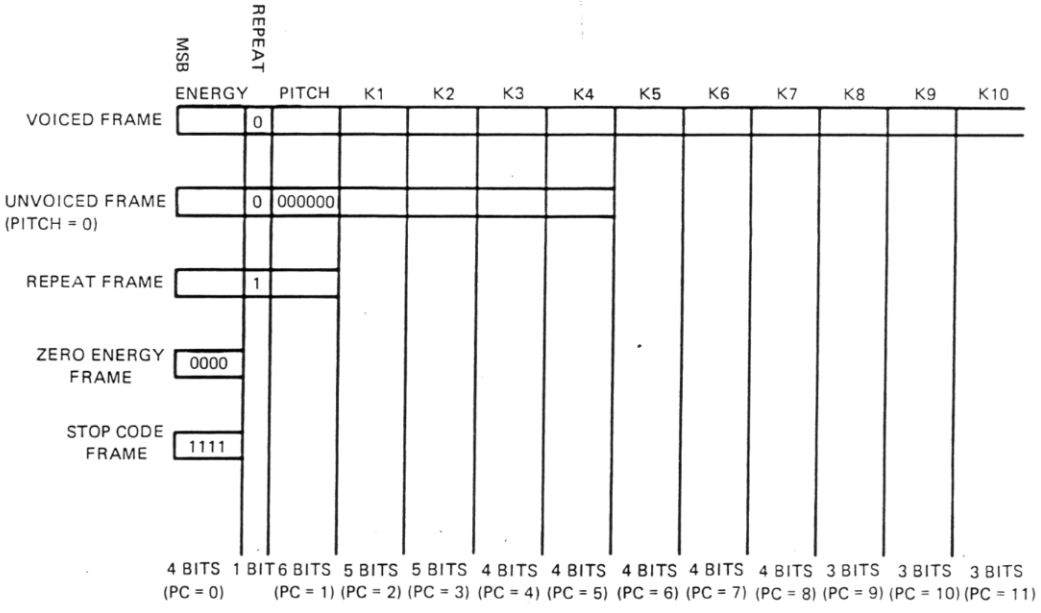


FIGURE 5 – FRAME DATA STRING LENGTHS

One complete set of parameters (12), used as target values during interpolation, is stored in coded form in the synthesizer. The storage medium is a 50-bit RAM of variable word length, e.g., six bits for pitch, three bits for K10. Data is supplied to the RAM via the parallel outputs of a serial shift register which accepts data from some VSM. The Parameter RAM outputs are used as inputs for the Parameter ROM.

8.2 D/A CONVERSION

The VSP contains an eight-bit digital-to-analog converter with 2% linearity LSB resolution. Every 125 microseconds the most-significant 10 bits of the 14-bit lattice filter output are sampled. From this sample, the seven low-order bits and the sign bit (MSB) are sent to the D/A converter. The remaining two bits are combined logically with the sign bit and used to clip the driver to either a full ON or full OFF condition. Table 4 shows the analog output from the D/A converter for various inputs from the lattice filter.

TABLE 4 – DIGITAL-TO-ANALOG CONVERTER OUTPUT

NO.	Y LATCH OUTPUT				D/A INPUT	ANALOG OUTPUT (μA)
	Y_{L13}	Y_{L12}	Y_{L11}	Y_{L10}–Y_{L4}		
	0	1	1	X	11111111	0
>+127	0	1	0	X	11111111	0
	0	0	1	X	11111111	0
127	0	0	0	1111111	11111111	0
126	0	0	0	1111110	11111110	5.86
			–			
			–			
			–			
+1	0	0	0	0000001	10000001	738
0	0	0	0	0000000	10000000	744
*–1	1	1	1	1111111	01111111	750
–2	1	1	1	1111110	01111110	755.8
			–			
			–			
			–			
–128	1	1	1	0000000	00000000	1500
<–128	1	1	0	X	00000000	1500
	1	0	1	X	00000000	1500
	1	0	0	X	00000000	1500

*No output, resting level.

8.3 AUDIO OUTPUT

The output of the D/A converter (see Table 4) is a current source designed to deliver 0 to 1.5 milliamperes with resolution to 5.9 microamperes. This output has been optimized to drive the EXT AUD input of the SN76489AN sound generator chip. With a 1.8-kilohm resistor in series, the VSP delivers 2.7 volts (I = 1.5 milliamperes) when the Y latch output is less than –128. When the Y latch output is greater than +127, the audio output is clipped to 0 volts. When no speech generation is taking place, the Y latch output is –1 making the audio output drive 750 microamperes. (Speaker output must be ac-coupled to audio amplifier).

9. ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Any pin with respect to V_{SS}	–20 V to +0.3 V
Power Dissipation	600 mW
Operating temperature range	0°C to 70°C
Storage temperature range	–30°C to 125°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

9.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}	4.5	5	5.5	V
Supply voltage, V_{REF}		0		V
Supply voltage, V_{DD}	–4.5	–5	–5.5	V
High-level input voltage, V_{IH}	V_{SS}–0.6		V_{SS}	V
Low-level input voltage, V_{IL} (see Note 1)		0	V_{SS}–4	V
Operating free-air temperature, T_A	0		70	°C
Operational frequency (External RC)	576	640	704	kHz

NOTE 1: The algebraic convention, where the more-positive (less-negative) limit is designated as maximum, is used in this data sheet for logic voltages levels only.

9.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

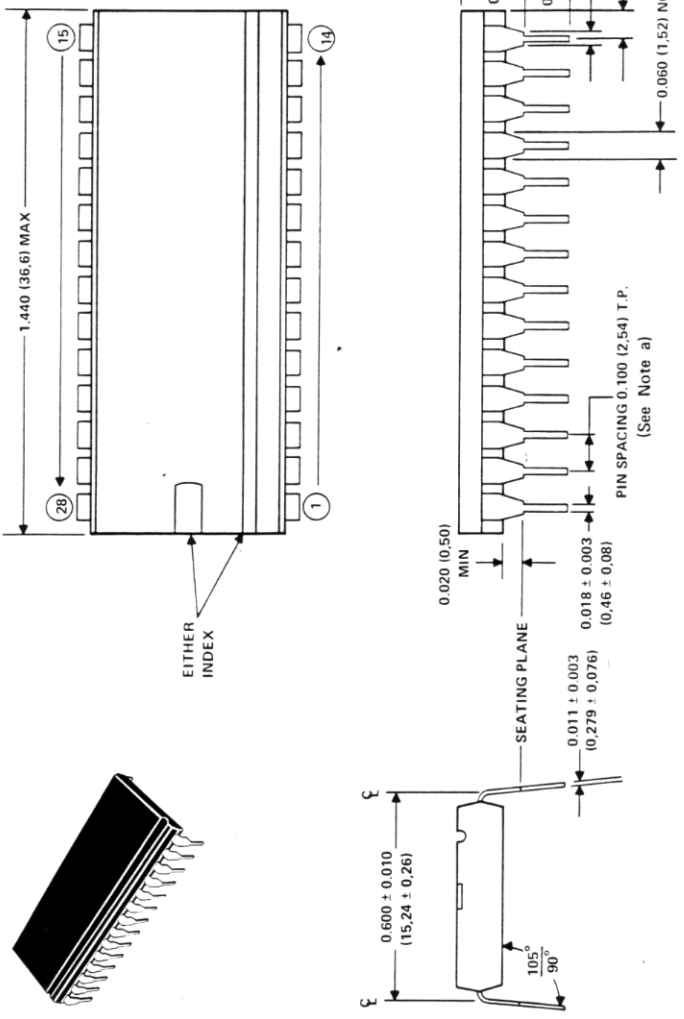
PARAMETER			MIN	TYP	MAX	UNIT
V_{OH}	D0-D7, $\overline{WS}$, $\overline{RS}$, $\overline{INT}$	I_{OH} = 0.4 mA	2.4		V_{SS}	V
	ROMCLK, ADD 1-8, M0, M1	I_{OH} = 100 µA	V_{SS}–0.5		V_{SS}	V
V_{OL}	D0-D7, $\overline{WS}$, $\overline{RS}$, $\overline{INT}$	I_{OL} = 1.6 mA	V_{RSF}–0.5	0	V_{RSF}+0.5	V
	ROMCLK, ADD 1-8, M0, M1	I_{OL} = 100 µA			V_{SS}–4.5	V
I_{REF}	Supply current from V_{REF}			3	5	mA
I_{DD}	Supply current from V_{DD}			10	35	mA
C_i	Input capacitance, (except data bus)			15		pF
C_o	Output capacitance, (except data bus)			15		pF
C_{db}	Data bus load capacitance		25		300	pF

9.4 STATIC DISCHARGE PROTECTION

All inputs and outputs are guarded against electrostatic damage by state-of-the-art protection devices incorporated on the chip.

11. MECHANICAL DATA

11.1 28-PIN 600-MIL PLASTIC PACKAGE (100-MIL PIN SPACING)

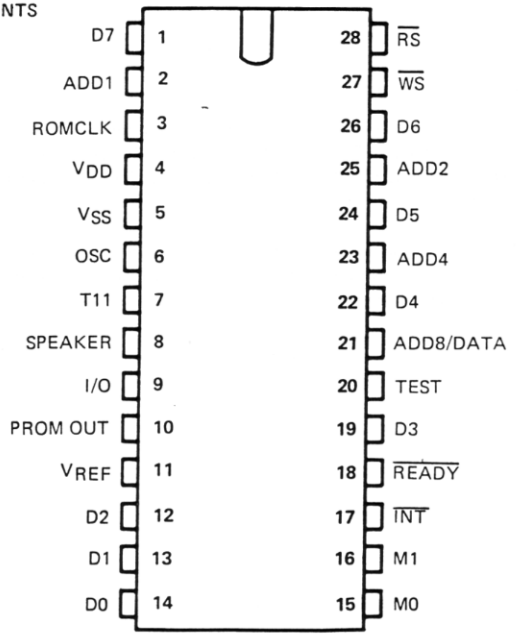


NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

11.2 PIN ASSIGNMENTS AND FUNCTIONS

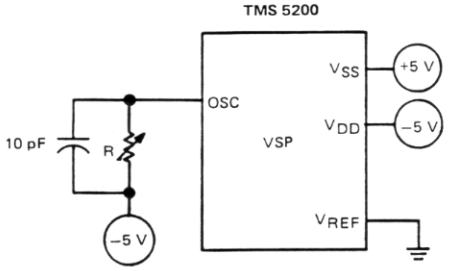
PIN	NAME	IN/OUT	FUNCTION
1	DBUS 7	I/O	Memory data bus (LSB)
2	ADD1	O	Address bus to VSM (LSB)
3	ROMCLK	O	Clock to VSM
4	V_{DD}	I	Drain supply voltage (−5 V NOM)
5	V_{SS}	I	Substrate supply voltage (+5 V NOM)
6	OSC	I	Oscillator input
7	T11	O	Sync
8	SPEAKER	O	Audio output
9	I/O	O	Serial data out
10	PROM OUT	O	Testing use only
11	V_{REF}	I	Ground reference voltage (0 V NOM)
12	DBUS 2	I/O	Memory data bus
13	DBUS 1	I/O	Memory data bus
14	DBUS 0	I/O	Memory data bus (MSB)
15	M0	O	Command bit 0 to VSM
16	$\overline{M1}$	O	Command bit 1 to VSM
17	$\overline{INT}$	O	Interrupt (active low)
18	$\overline{READY}$	O	Transfer cycle W/CPU complete
19	DBUS 3	I/O	Memory data bus
20	TEST	I	Testing use only
21	ADD8/DATA	I/O	Address to VSM and serial data in (MSB)
22	DBUS 4	I/O	Memory data bus
23	ADD 4	O	Address bus to VSM
24	DBUS 5	I/O	Memory data bus
25	ADD 2	O	Address bus to VSM
26	DBUS 6	I/O	Memory data bus
27	$\overline{WS}$	I	Write select (active low)
28	$\overline{RS}$	I	Read select (active low)

11.3 TERMINAL ASSIGNMENTS



APPENDIX A

SYSTEM CLOCK



RC OPTION

TYPICAL VALUES:

SAMPLE FREQUENCY	R
10 kHz	R = 80-100 kΩ
8 kHz	R = 120-200 kΩ

FIGURE A-1 – TMS 5200 OSCILLATOR OPTIONS

A.1 OSCILLATOR TRIMMING PROCEDURE

To avoid capacitive loading of the high impedance OSC input, the following procedure is recommended for setting the TMS 5220 clock frequency. Reference to Table A-1, Comparison of System Times (page 16), shows that an RC oscillator frequency of 640 kHz corresponds to a ROM clock rate of 160 kHz. This signal is buffered and not affected by measurement instrument capacities.

To set the RC oscillator frequency, connect a frequency counter to the ROM clock output of the TMS 5220 and trim the reading to 160 kHz. Use of 10 pF shunt capacitor is recommended to prevent circuit layout and environmental stray noise from affecting device operation.

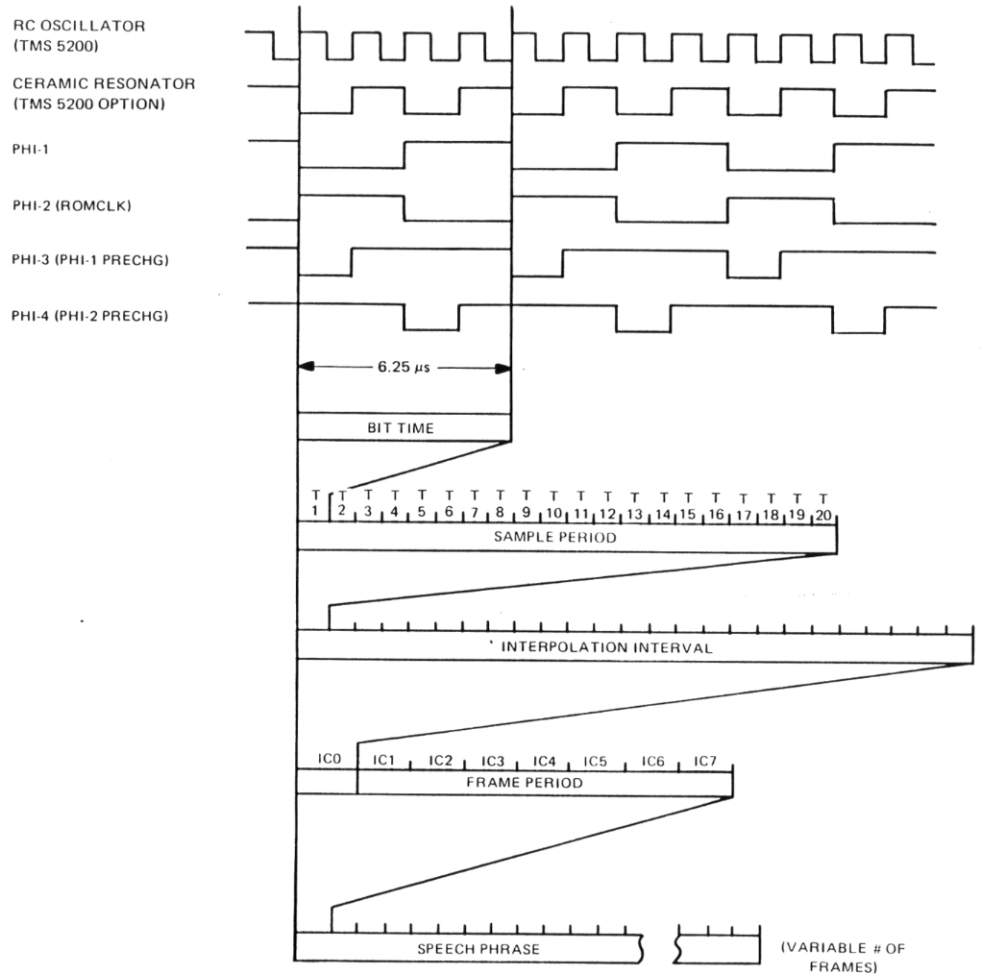


FIGURE A-2 – SYSTEM TIMING SUMMARY

TABLE A-1 – A COMPARISON OF SYSTEM TIMES

SAMPLE RATE:	10 kHz	8 kHz
FRAME RATE	50 Hz	40 Hz
FRAME PERIOD	20 ms	25 ms
INTERPOLATION RATE	400 Hz	320 Hz
INTERPOLATION INTERVAL	2.5 ms	3.125 ms
SAMPLE RATE	10 kHz	8 kHz
SAMPLE PERIOD	100 μs	125 μs
ROM CLOCK RATE	200 kHz	160 kHz
ROM CLOCK PERIOD	5 μs	6.25 μs
RC OSC RATE	800 kHz	640 kHz
RC OSC PERIOD	1250 ns	1562.5 ns

NOTE: All timing references in this data manual are based on an 8-kHz sample rate.

APPENDIX B
TMS 5220 INTERNAL COMMAND EXECUTION

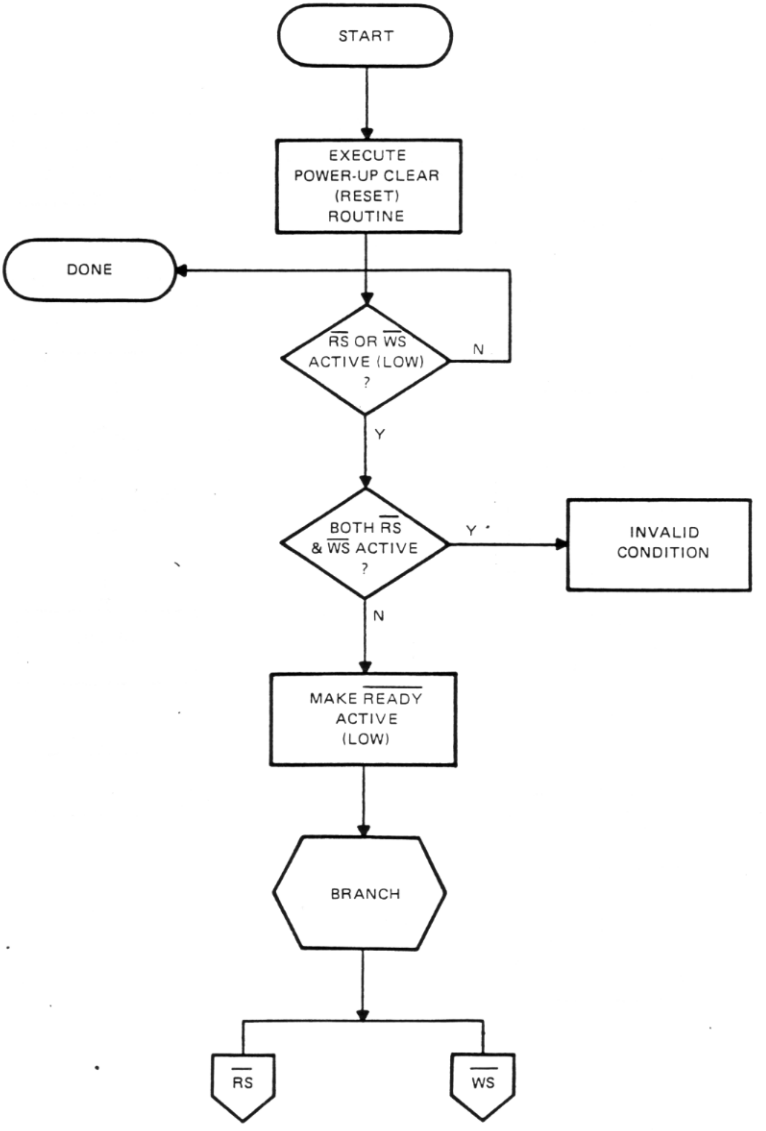


FIGURE B-1 – POWER ON

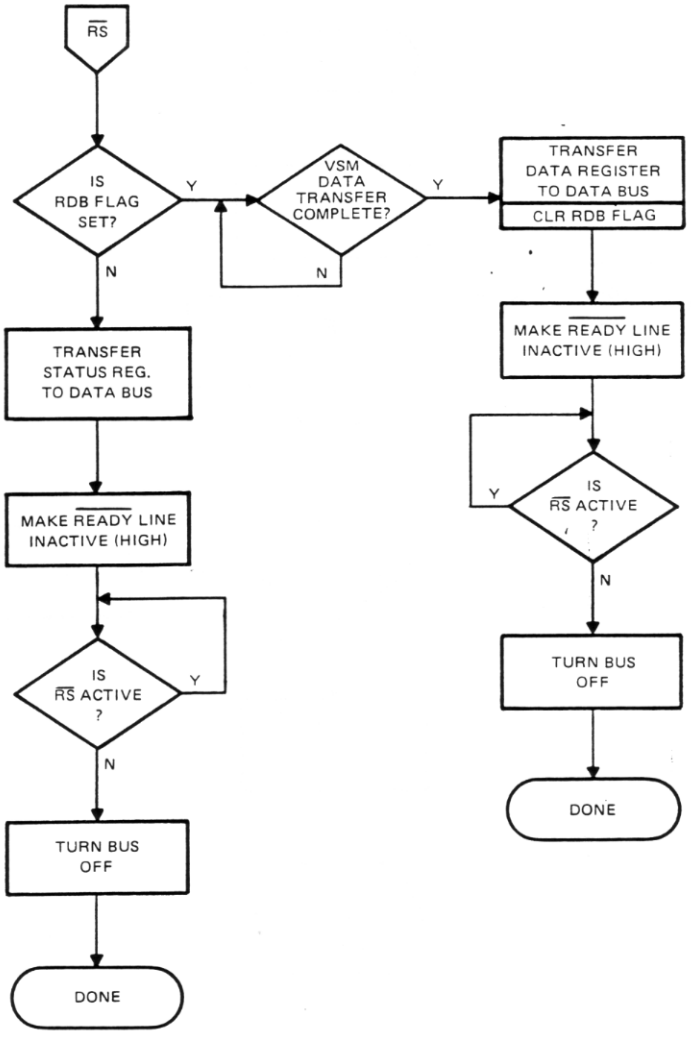


FIGURE B-2 – READ SELECT ACTIVE

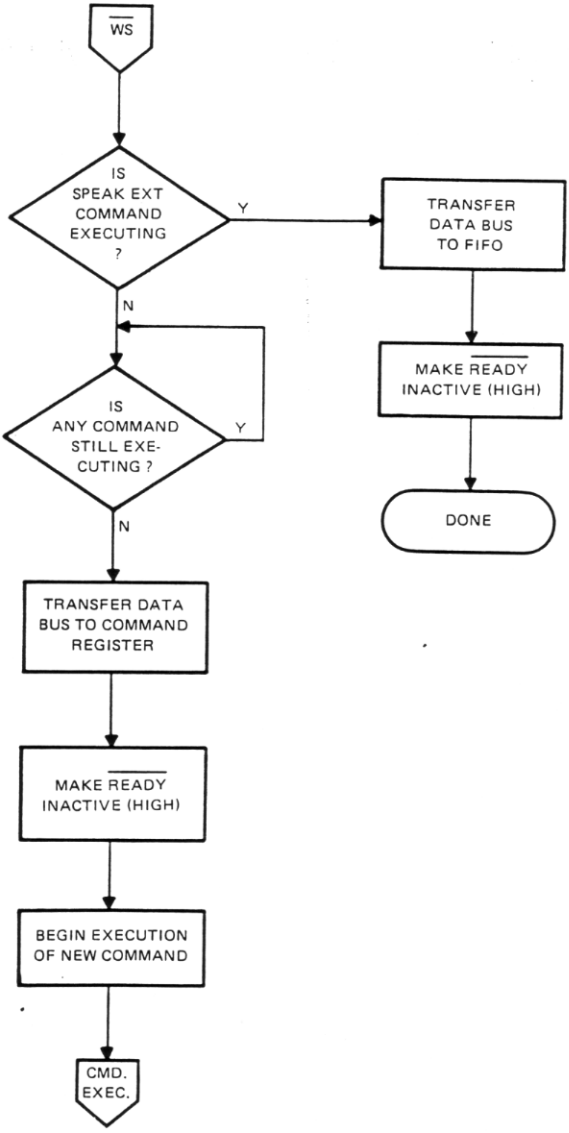


FIGURE B-3 – WRITE SELECT ACTIVE

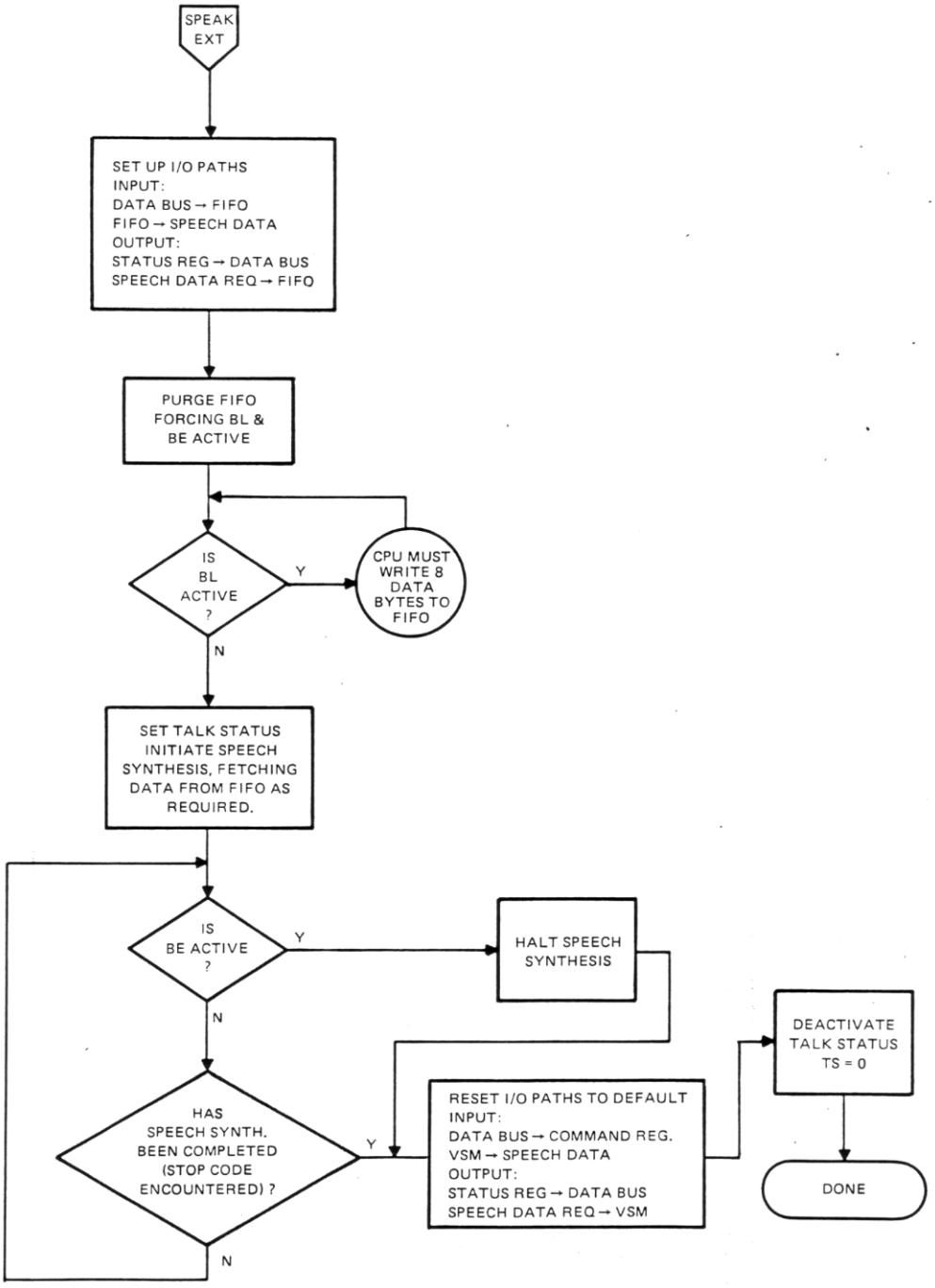


FIGURE B-4 – SPEAK EXTERNAL COMMAND

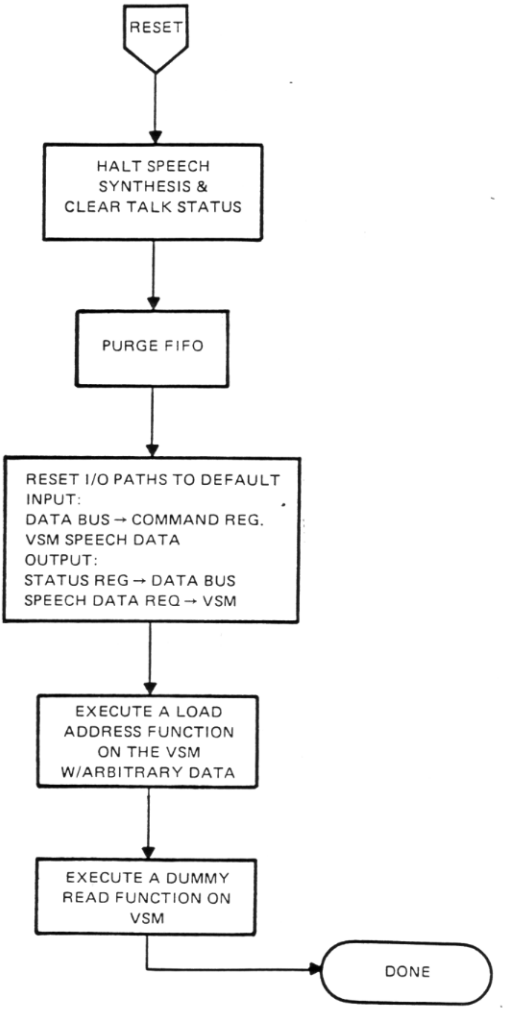


FIGURE B-5 – RESET COMMAND

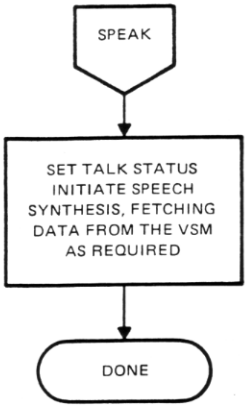


FIGURE B-6 – SPEAK

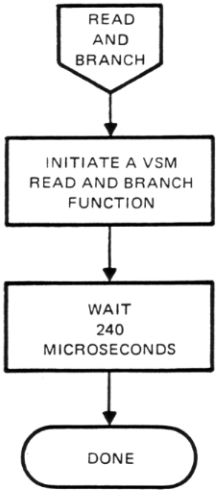


FIGURE B-7 – READ AND BRANCH

APPENDIX C

SYSTEM TIMING DIAGRAMS

Write Cycle for Read and Branch, Load Address, Speak, Speak External and Reset Commands

timing requirements

PARAMETER			MIN	NOM	MAX	UNIT
t_{WSL-DV}	Delay time from $\overline{WS}$ low to data valid				7	μs
t_{RL-DX}	Delay time from $\overline{READY}$ low to data invalid		0			μs
t_{RH-WSH}	Delay time from $\overline{READY}$ high to $\overline{WS}$ high		6			μs
t_{wait}	Read-and-branch command wait time from $\overline{READY}$ high until next allowable* command				595	μs
t_{wait}	Load-address command wait time from $\overline{READY}$ high until next allowable* command				42	μs
t_{wait}	Speak command wait time from $\overline{READY}$ high until next allowable* command	Preceded by load-address command			287	μs
		Not preceded by load-address command	56			
t_{wait}	Reset command wait time from $\overline{READY}$ high until next allowable* command				300	μs
t_{wait}	Speak external command wait time from $\overline{READY}$ high until next allowable* command				42	μs

switching characteristics

PARAMETER		MIN	NOM	MAX	UNIT
t_{WSL-RH}	Delay time from $\overline{WS}$ low to $\overline{READY}$ high			100	ns
$t_{w(R)}$	$\overline{READY}$ high pulse width	18		26	μs

All timing is based on a clock frequency of 8 kHz.

* If a new command is issued prior to the completion of the present command (before the end of t_{wait}), then the $\overline{READY}$ signal will go high and stay high until the present command is finished executing in the VSP.

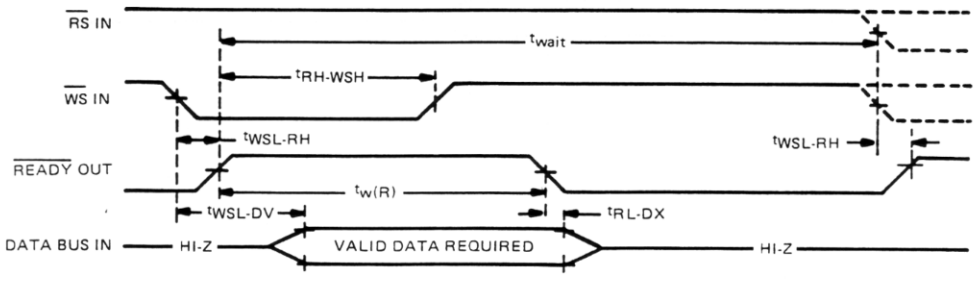


FIGURE C-1

WRITE CYCLE FOR EXTERNAL SPEECH DATA

timing requirements

	PARAMETER	MIN	NOM	MAX	UNIT
t_{WSL-DV}	Delay time from $\overline{WS}$ low to data valid			7	μs
t_{RL-DX}	Delay time from $\overline{READY}$ low to data invalid	0			μs
t_{RH-WSH}	Delay time from $\overline{READY}$ high to $\overline{WS}$ high	6			μs
t_{wait}	Wait time from $\overline{WS}$ high until next allowable* access	10			μs

switching characteristics

	PARAMETER	MIN	TYP	MAX	UNIT
t_{WSL-RH}	Delay time from $\overline{WS}$ low to $\overline{READY}$ high			100	ns
$t_{w(R)}$	$\overline{READY}$ high pulse width			23	μs

All timing is based on a clock frequency of 8 kHz.

* If a new command is issued to the VSP prior to the completion of the present command then the $\overline{READY}$ command will go high (as usual) and remain high until the completion of the present command as defined by t_{wait} above.

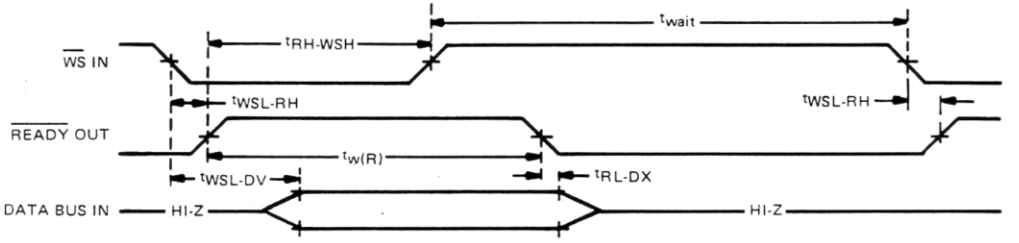


FIGURE C-2

READ CYCLE FOR STATUS TRANSFERS

timing requirements

	PARAMETER	MIN	NOM	MAX	UNIT
t_{RH-RSH}	Delay time from $\overline{READY}$ high to $\overline{RS}$ high	6			μs
t_{wait}	Wait time from $\overline{RS}$ high to next allowable* command	12			μs

switching characteristics

	PARAMETER	MIN	TYP	MAX	UNIT
t_{RSL-RH}	Delay time from $\overline{RS}$ low to $\overline{READY}$ high			100	ns
t_{RH-DV}	Delay time from $\overline{READY}$ high to data valid (stable)	6		11	μs
t_{RSL-DX}	Delay time from $\overline{RS}$ low to data bus driven (output unstable)		$t_{RH-DV}-2$		μs
t_{RSH-DZ}	Delay time from $\overline{RS}$ high to data output disabled			10.5	μs

* If a new command is issued to the VSP prior to the completion of the present command, then after the $\overline{READY}$ signal goes high, in its normal response time, it will remain high until the present command has been fully executed by the VSP.

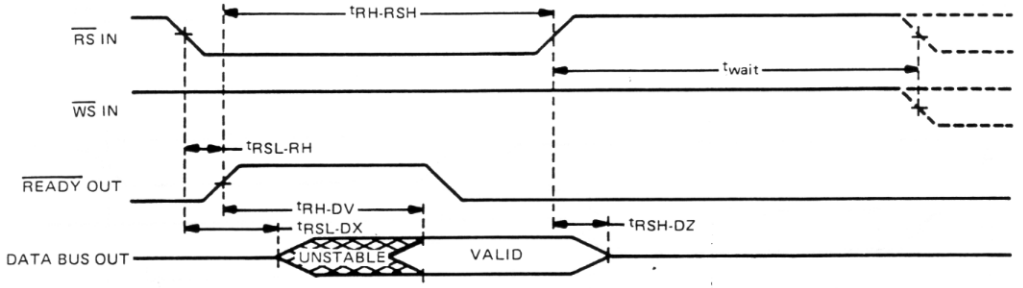


FIGURE C-3

READ BYTE SEQUENCE

timing requirements

PARAMETER		MIN	NOM	MAX	UNIT
t_{WSL-DV}	Delay time from $\overline{WS}$ low to data valid			7	μs
t_{RH-WSH}	Delay time from $\overline{READY}$ high to $\overline{WS}$ high	6			μs
t_{WSH-DX}	Delay time from $\overline{WS}$ high to data invalid	0			μs
t_{RH-RSH}	Delay time from $\overline{READY}$ high to $\overline{RS}$ high	8			μs
$t_{WSH-RSL}$	Delay time from $\overline{WS}$ high to $\overline{RS}$ low	12			μs

switching characteristics

PARAMETER			MIN	TYP	MAX	UNIT
t_{WSL-RH}	Delay time from $\overline{WS}$ low to $\overline{READY}$ high				100	ns
t_{RSL-RH}	Delay time from $\overline{RS}$ low to $\overline{READY}$ high				100	ns
$t_{w(R)}$	$\overline{READY}$ high pulse width (write)				26	μs
t_{RL-RL}	Delay time from $\overline{READY}$ low (write) to $\overline{READY}$ low (read)	No previous load address			320	μs
		Previous load address			440	
t_{RSH-DZ}	Delay time from $\overline{RS}$ high to data output disabled		4		9	μs

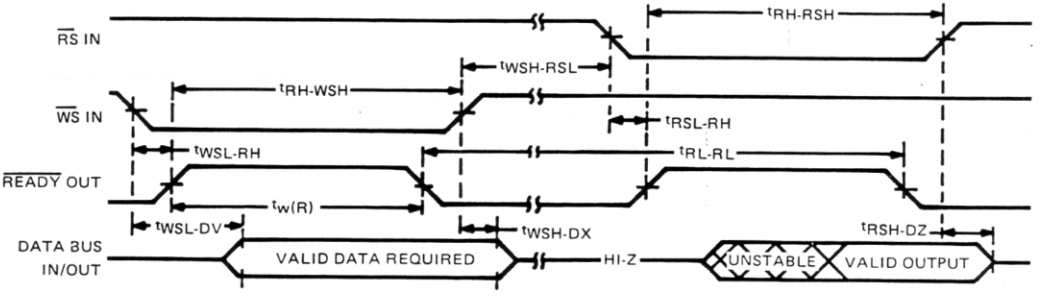


FIGURE C-4

TMS 5220 CODING TABLE

RMS	PITCH	K(1)	K(2)	K(3)	K(4)	K(5)	K(6)	K(7)	K(8)	K(9)	K(10)
0	0	−0.97850	−0.64000	−0.86000	−0.64000	−0.64000	−0.50000	−0.60000	−0.50000	−0.50000	−0.40000
52	15	−0.97270	−0.58999	−0.75467	−0.53145	−0.54933	−0.41333	−0.50667	−0.31429	−0.34286	−0.25714
87	16	−0.97070	−0.53500	−0.64933	−0.42289	−0.45867	−0.32667	−0.41333	−0.12857	−0.18571	−0.11429
123	17	−0.96680	−0.47507	−0.54400	−0.31434	−0.36800	−0.24000	−0.32000	0.05714	−0.02857	0.02857
174	18	−0.96290	−0.41039	−0.43867	−0.20579	−0.27733	−0.15333	−0.22667	0.24286	0.12857	0.17143
246	19	−0.95900	−0.34129	−0.33333	−0.09723	−0.18667	−0.06667	−0.13333	0.42857	0.28571	0.31429
348	20	−0.95310	−0.26830	−0.22800	0.01132	−0.09600	0.02000	−0.04000	0.61429	0.44286	0.45714
491	21	−0.94140	−0.19209	−0.12267	0.11987	−0.00533	0.10667	0.05333	0.80000	0.60000	0.60000
694	22	−0.93360	−0.11350	−0.01733	0.22843	0.08533	0.19333	0.14667			
981	23	−0.92580	−0.03345	0.08800	0.33698	0.17600	0.28000	0.24000			
1385	24	−0.91600	0.04702	0.19333	0.44553	0.26667	0.36667	0.33333			
1957	25	−0.90620	0.12690	0.29867	0.55409	0.35733	0.45333	0.42667			
2764	26	−0.89650	0.20515	0.40400	0.66264	0.44800	0.54000	0.52000			
3904	27	−0.88280	0.28087	0.50933	0.77119	0.53867	0.62667	0.61333			
5514	28	−0.86910	0.35325	0.61467	0.87975	0.62933	0.71333	0.70667			
7789	29	−0.85350	0.42163	0.72000	0.98830	0.72000	0.80000	0.80000			
	30	−0.80420	0.48553								
	31	−0.74058	0.54464								
	32	−0.66019	0.59878								
	33	−0.56116	0.64796								
	34	−0.44296	0.69227								
	35	−0.30706	0.73190								
	36	−0.15735	0.76714								
	37	−0.00005	0.79828								
	38	0.15725	0.82567								
	39	0.30696	0.84965								
	40	0.44288	0.87057								
	41	0.56109	0.88875								
	42	0.66013	0.90451								
	44	0.74054	0.91813								
	46	0.80416	0.92988								
	48	0.85350	0.98830								
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