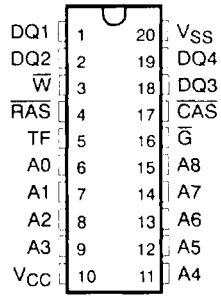
This data sheet is applicable to all TMS44C256s symbolized with Revision "D" and subsequent revisions as described on page 5-21.

- **262 144 × 4 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

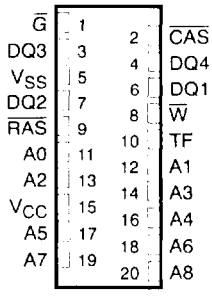
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44C256-60	60 ns	15 ns	30 ns	110 ns
TMS44C256-70	70 ns	18 ns	35 ns	130 ns
TMS44C256-80	80 ns	20 ns	40 ns	150 ns
TMS44C256-10	100 ns	25 ns	45 ns	180 ns
TMS44C256-12	120 ns	30 ns	55 ns	220 ns

- **Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs and Clocks Are TTL Compatible**
- **High-Reliability Plastic 20-Pin 300-Mil-Wide DIP, 20/26 J-Lead Surface Mount (SOJ) ('44C256-60 and '44C256-70 Available in SOJ Only), 20/26 J-Lead Thin Surface Mount (ThinSOJ), or 20-Pin Zig-Zag In-Line (ZIP) Packages**
- **Operation of TI's Megabit CMOS DRAMs Can Be Controlled by TI's SN74ALS6301 and SN74ALS6302 Dynamic RAM Controllers**
- **Operating Free-Air Temperature . . . 0°C to 70°C**

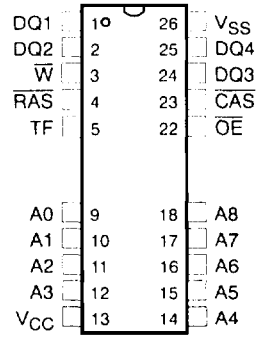
N Package
(Top View)



SD Package
(Top View)



DJ and DN Packages†
(Top View)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data-Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44C256 series are high-speed, 1 048 576-bit dynamic random access memories, organized as 262 144 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at low cost.

EPIC is a trademark of Texas Instruments Incorporated

description (continued)

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 305 mW operating and 11 mW standby on 120 ns devices.

The EPIC technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a – 1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44C256 is offered in a 20-pin dual-in-line (N suffix) package, a 20-pin zig-zag in-line (SD suffix) package, a 20/26 J-lead plastic surface mount SOJ (DJ suffix), and a 20/26 J-lead thin plastic surface mount SOJ (DN suffix). The TMS44C256-60 and TMS44C256-70 are available in the 20/26 J-lead plastic surface mount SOJ (DJ suffix) only. These packages are guaranteed for operation from 0°C to 70°C.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44C256 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after $t_{h(RA)}$ (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting a write operation with $\overline{G}$ grounded.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high-impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying $t_{d(GHD)}$.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

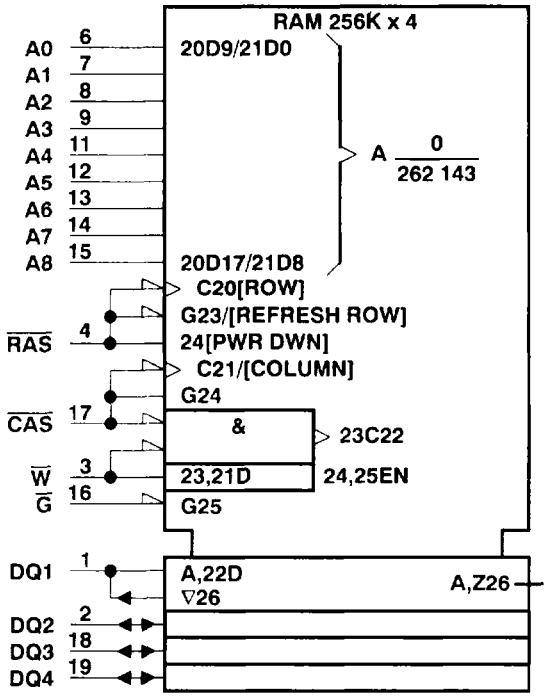
power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level.

test function pin

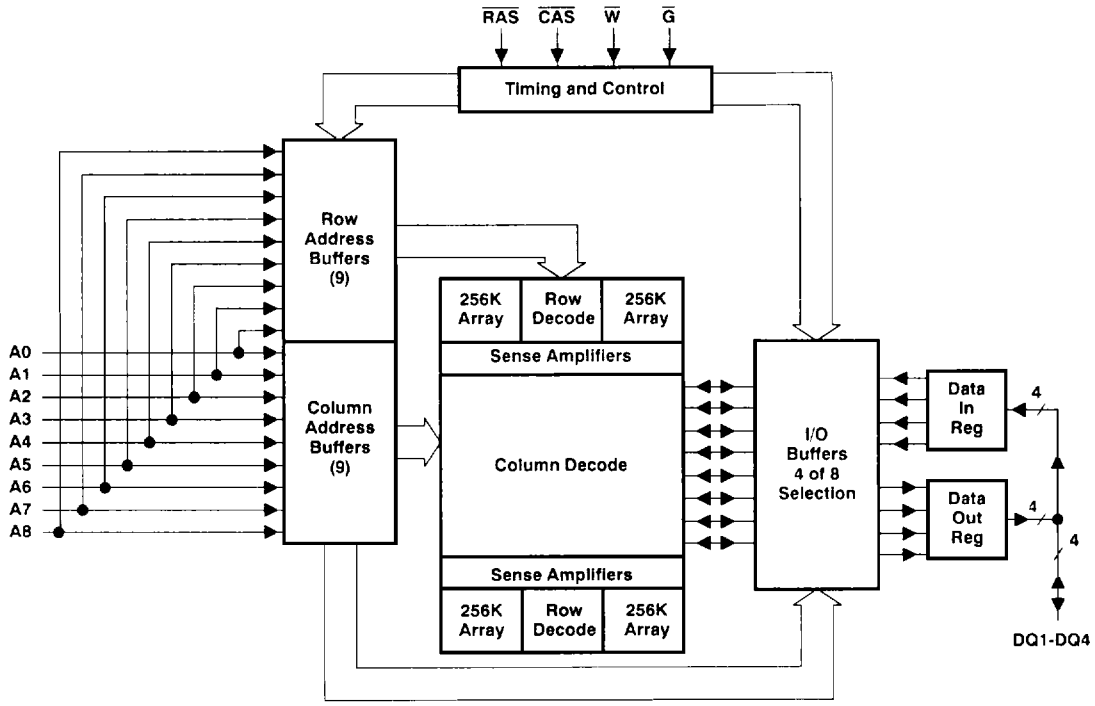
During normal device operation the TF pin must either be disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Voltage range on V_{CC} . . . . . – 1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10	µA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		95		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2	mA
I_{CC3}	Average refresh circuit ($\overline{RAS}$-only, or CBR)	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		90		80	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60	mA

PARAMETER		TEST CONDITIONS	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		75		65		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2		2	mA
I_{CC3}	Average refresh circuit ($\overline{RAS}$-only, or CBR)	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		70		60		50	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		45		35	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			5	pF
$C_{i(W)}$	Input capacitance, write-enable input			5	pF
$C_{i(G)}$	Input capacitance, output-enable input			5	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		ALT. SYMBOL	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		15		18	ns
$t_{a(CA)}$	Access time from column-address	t_{CAA}		30		35	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		60		70	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		15		18	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		35		40	ns
$t_{d(CLZ)}$	$\overline{CAS}$ low to output in low Z	t_{CLZ}	0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	15	0	18	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}	0	15	0	18	ns

PARAMETER		ALT. SYMBOL	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		20		25		30	ns
$t_{a(CA)}$	Access time from column-address	t_{CAA}		40		45		55	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		80		100		120	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		20		25		30	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		40		50		60	ns
$t_{d(CLZ)}$	$\overline{CAS}$ low to output in low Z	t_{CLZ}	0		0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	20	0	25	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}	0	20	0	25	0	30	ns

NOTE 4: $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		ALT. SYMBOL	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	110		130		ns
$t_{c(W)}$	Write cycle time	t_{WC}	110		130		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	155		181		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	40		45		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	85		96		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	15	10 000	18	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	40		50		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	60	10 000	70	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	60	100 000	70	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	15		18		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	15		18		ns
$t_{h(CA)}$	Column-address hold time after $\overline{RAS}$ low	t_{CAH}	10		15		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	10		10		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	50		55		ns

Continued next page.

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$]).
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$]).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		ALT. SYMBOL	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	150		180		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	150		180		220		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	205		245		295		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	50		55		65		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	100		120		135		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	30	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		70		90		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100 000	100	100 000	120	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		20		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		30		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		30		ns
$t_{h(CA)}$	Column-address hold time after $\overline{RAS}$ low	t_{CAH}	15		20		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	12		15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		ns

Continued next page.

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$]).
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$]).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		ALT. SYMBOL	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 10)	t_{DH}	10		15		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	50		55		ns
$t_{h(WLGL)}$	$\overline{G}$ hold time after $\overline{W}$ low	t_{GH}	15		18		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 13)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 13)	t_{RRH}	0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		15		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	50		55		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	60		70		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	15		18		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	t_{CWD}	40		46		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	t_{RCD}	20	45	20	52	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	t_{RAD}	15	30	15	35	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	30		35		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	30		35		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	t_{RWD}	85		98		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 14)	t_{AWD}	55		63		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	15		18		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	10		10		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	15		15		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

Continued next page.

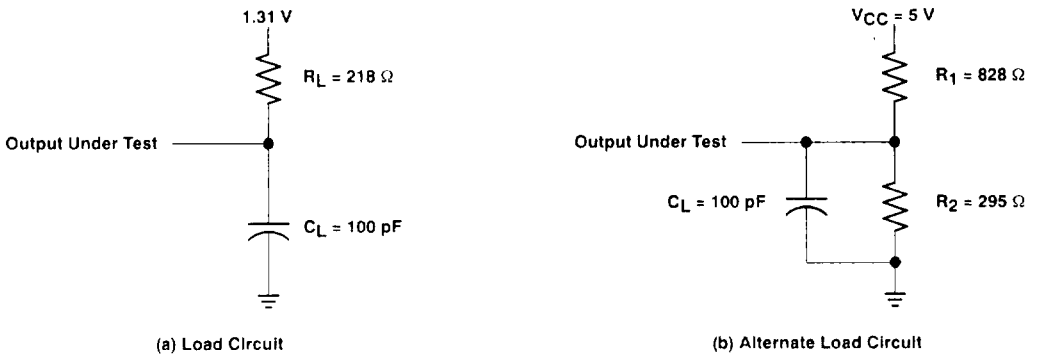
NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Read-modify-write operation only.
15. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		ALT. SYMBOL	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 10)	t_{DH}	15		20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		ns
$t_{h(WLGL)}$	$\overline{G}$ hold time after $\overline{W}$ low	t_{GH}	20		25		30		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 13)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 13)	t_{RRH}	0		0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	60		70		85		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	t_{CWD}	50		60		70		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	t_{RCD}	22	60	25	75	25	90	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	t_{RAD}	17	40	20	55	20	65	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	40		45		55		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	40		45		55		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	t_{RWD}	110		135		160		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 14)	t_{AWD}	70		80		95		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	20		25		30		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	10		10		10		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle
14. Read-modify-write operation only.
15. Maximum value specified only to guarantee access time
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

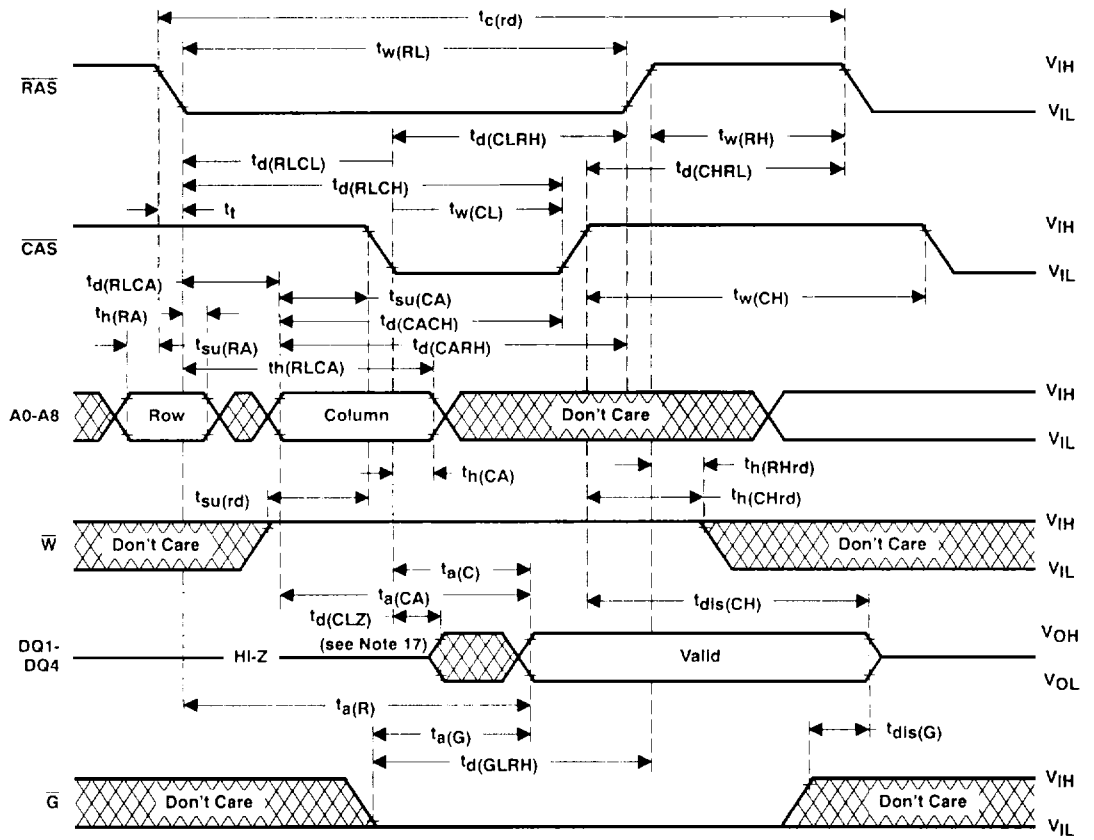
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

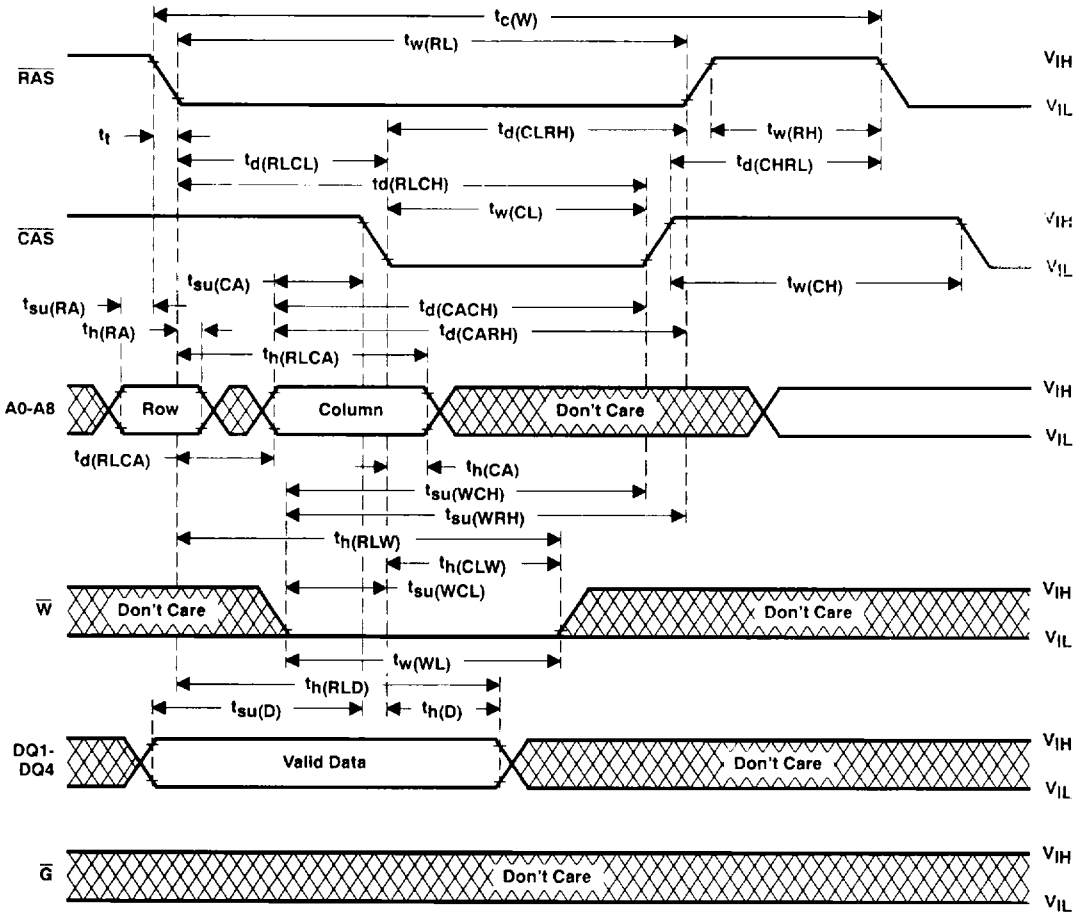
Figure 1. Load Circuits for Timing Parameters

read cycle timing

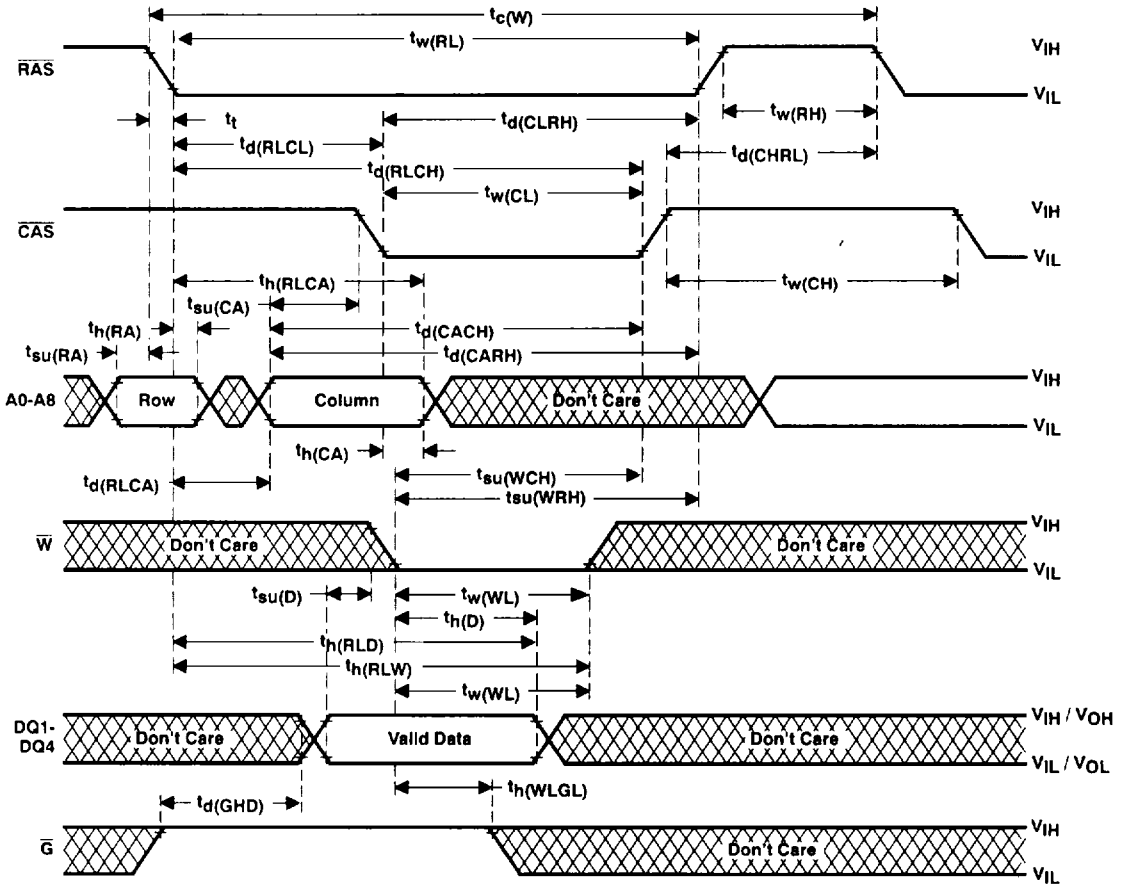


NOTE 17: Output may go from high-impedance to an invalid data state prior to the specified access time.

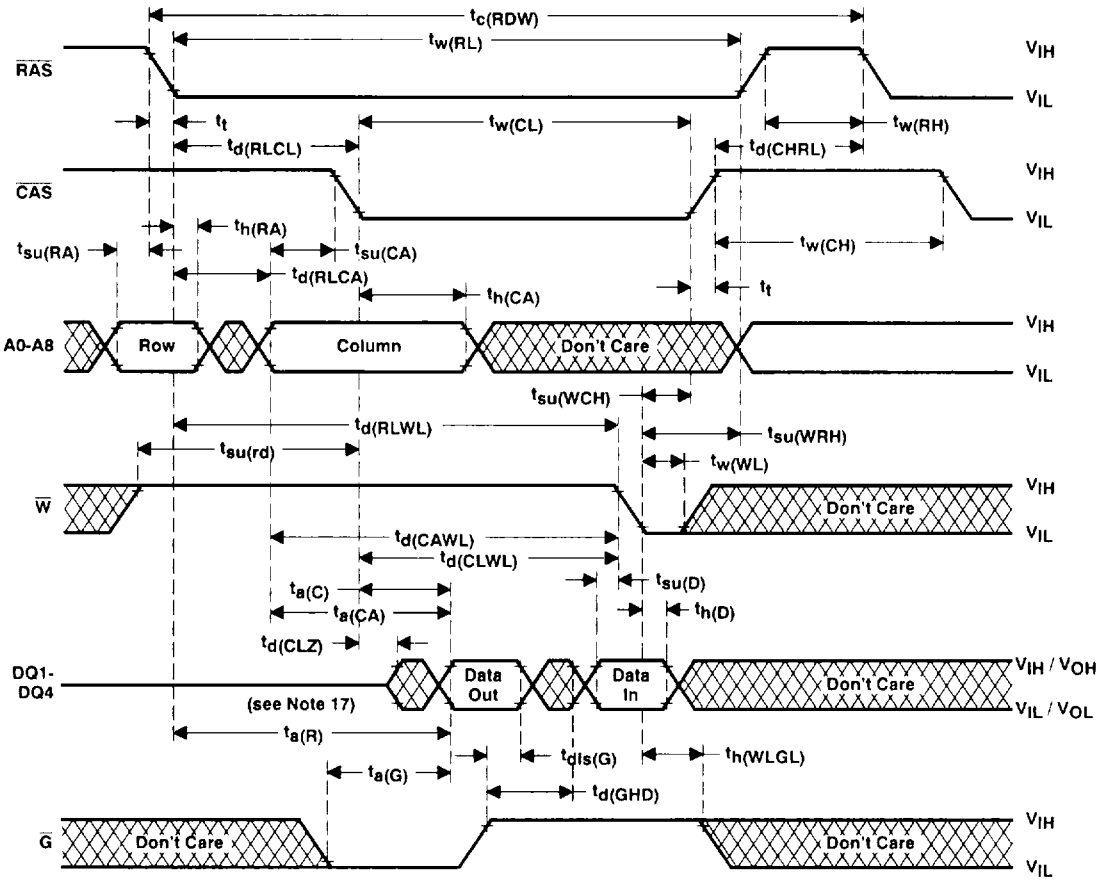
early write cycle timing



late write cycle timing

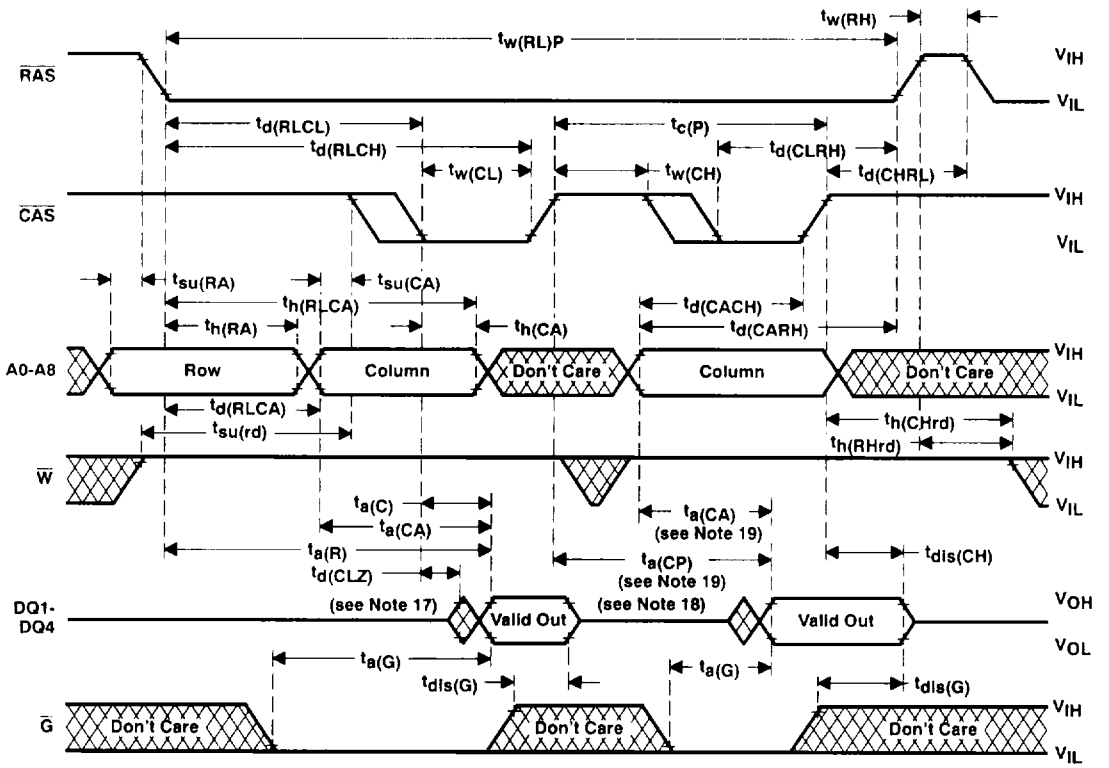


read-write/read-modify-write cycle timing



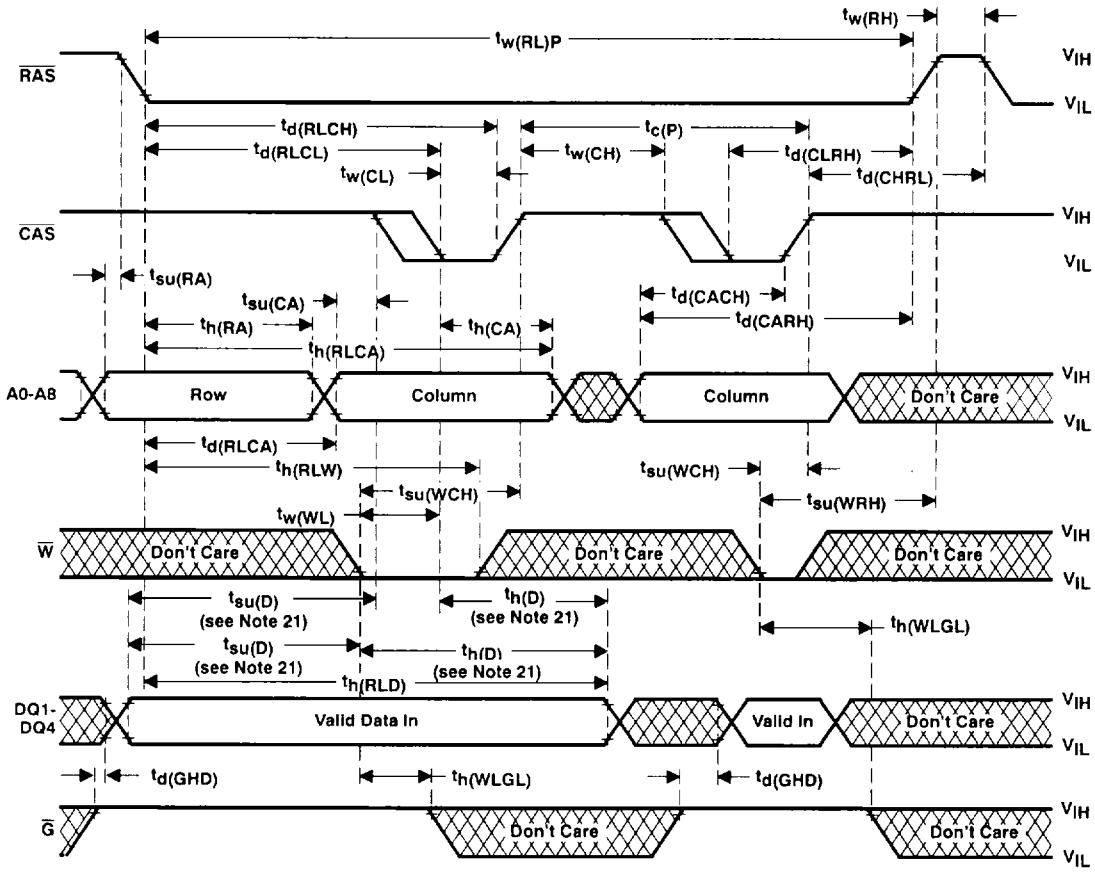
NOTE 17: Output may go from high-impedance to an invalid data state prior to the specified access time.

enhanced page-mode read cycle timing



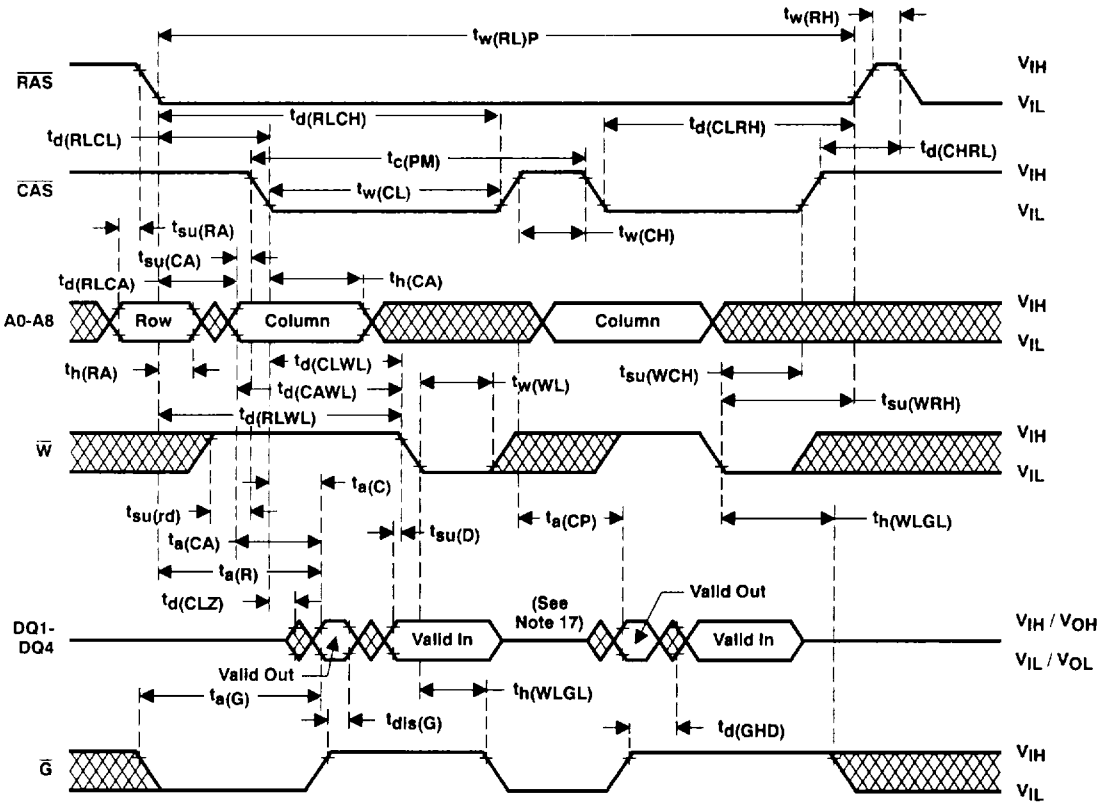
NOTES: 17. Output may go from high-impedance to an invalid data state prior to the specified access time.
18. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
19. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

enhanced page-mode write cycle timing



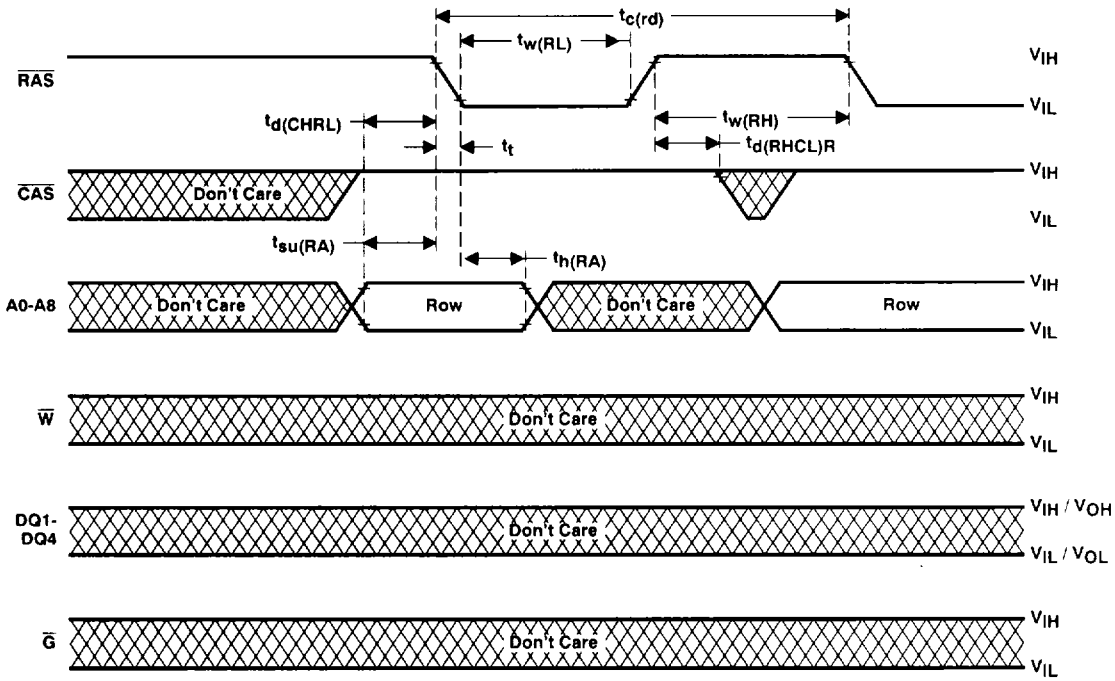
NOTES: 20. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
21. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing

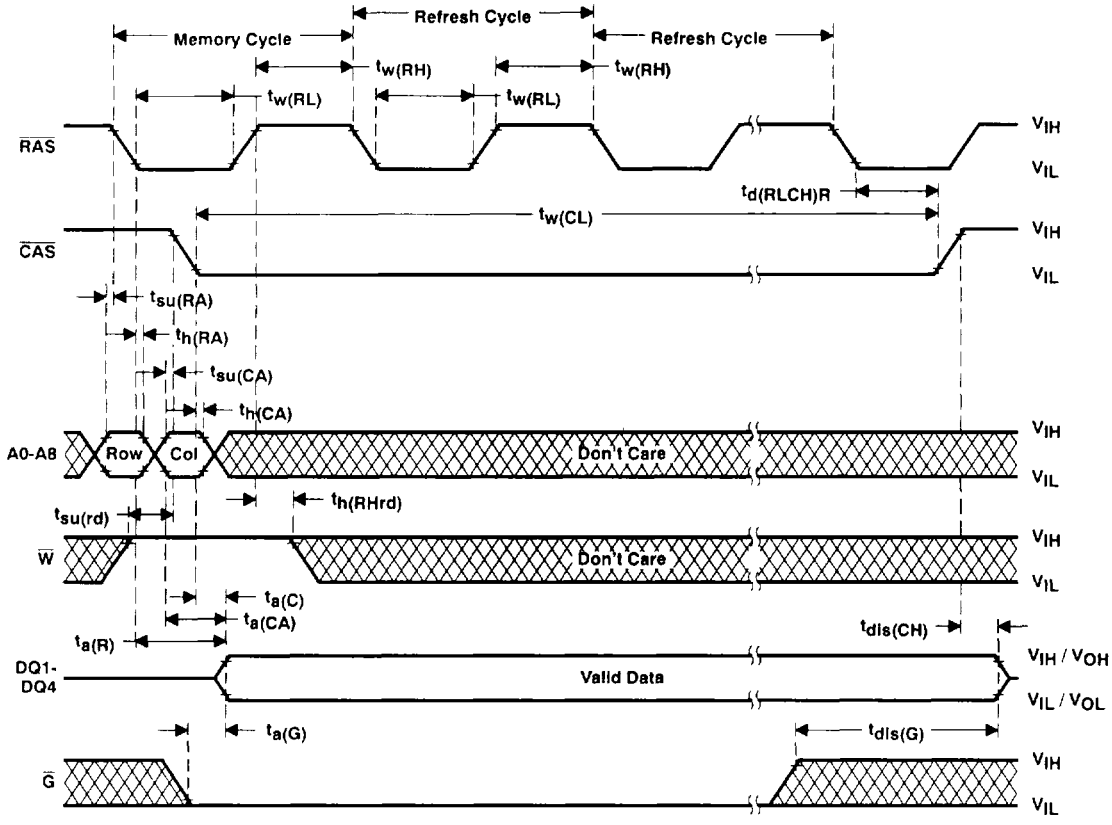


NOTES: 17. Output may go from high-impedance to an invalid data state prior to the specified access time.
22. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



hidden refresh cycle (enhanced page mode)



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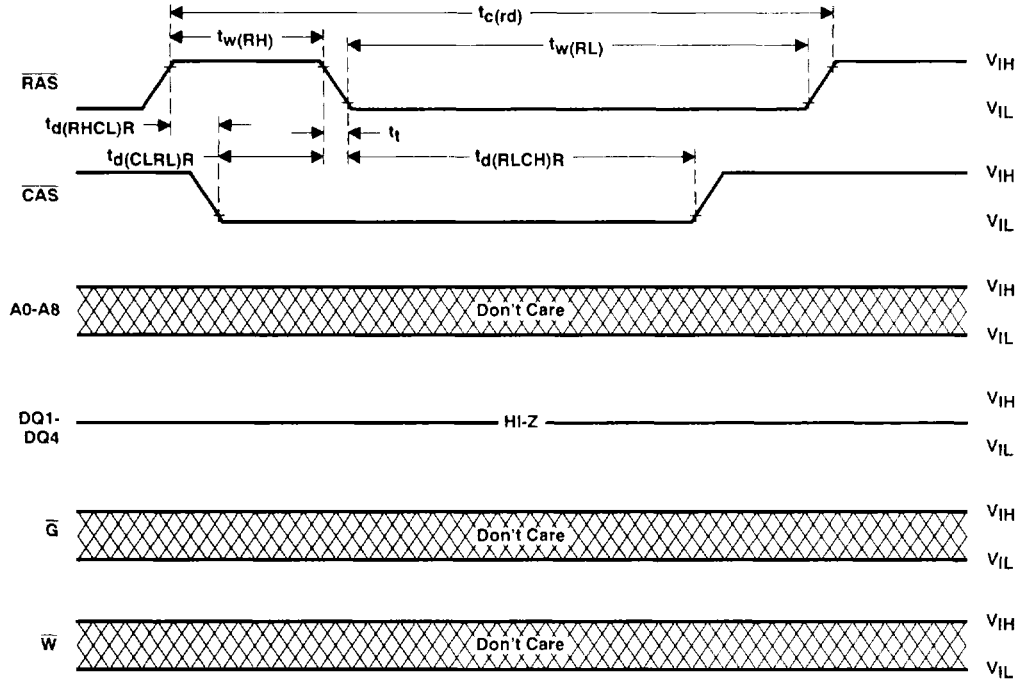
automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



device symbolization