OPTiFM™ Plug-and-Play Audio Controller

1.0 Overview

The OPTi 82C925 is a highly integrated digital audio controller for PC sound applications. The 82C925 is a replacement for the OPTi 82C924 audio controller that combines all of the features of the 82C924 along with built-in advanced OPTiFM™ synthesis technology.

The Plug-and-Play (PnP) standard minimized device conflicts by allowing the I/O address, IRQ and DMA settings to be allocated automatically from available system resources, rather than being selected by the user. Either the system BIOS, if it supports PnP, or the operating system maps the various logical devices within the 82C925 into the host system address space, as well as configuring the DMA and IRQ settings.

The 82C925 supports six logical devices: audio devices, including Sound Blaster™ Pro, Windows Sound System™ and FM Synthesis; game port; MPU-401 MIDI interface, IDE CD-ROM interface; modem interface; and 82C925 master control.

The 82C925 also provides push-button volume control, modem interface, and external serial EEPROM for further customization.

The 82C925 16-Bit Sound Controller provides all of the digital functions and interfaces for Sound Blaster Pro-compatible and Microsoft Windows Sound System-compatible cards. The 82C925 is intended to provide an integrated audio solution for business audio, educational/entertainment sound and multimedia applications.

Figure 1-1 System Block Diagram

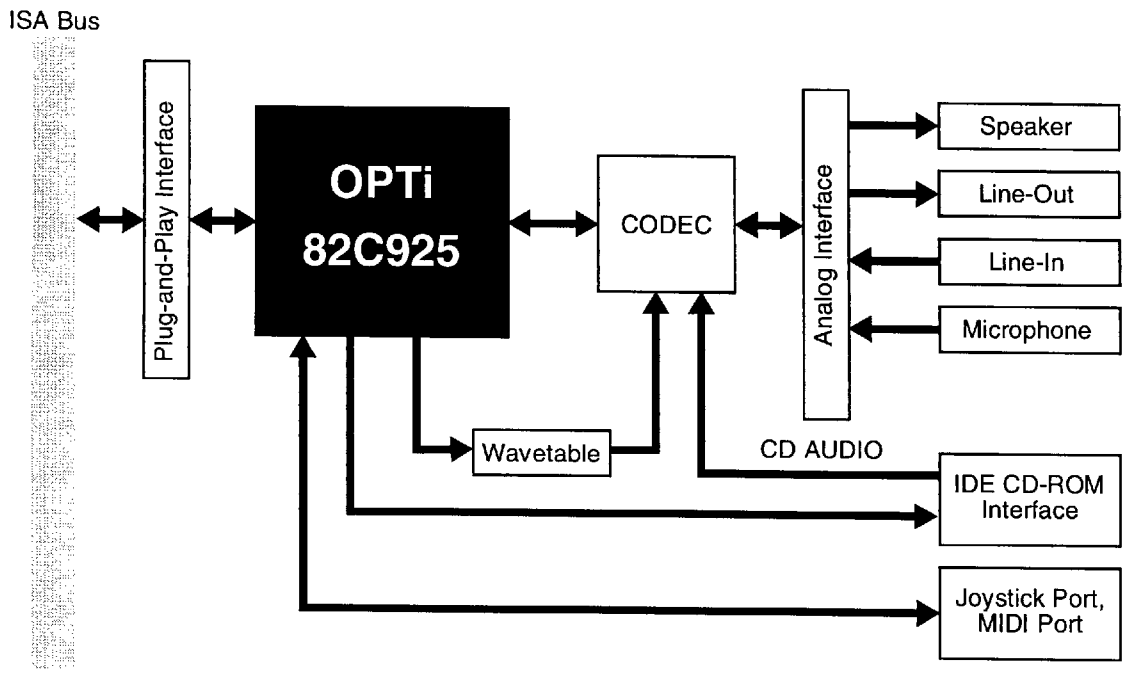
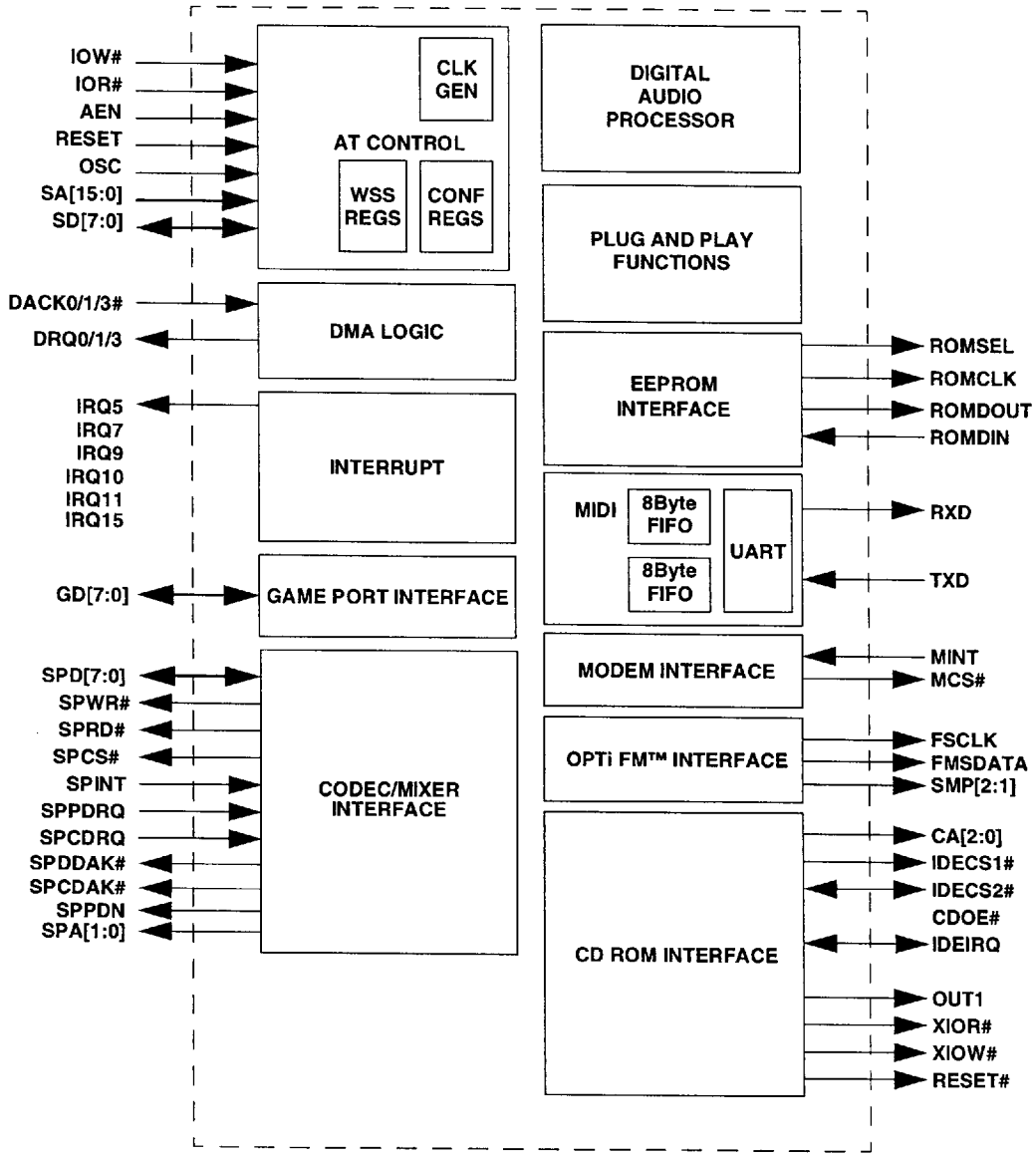


Figure 1-2 Functional Block Diagram



2.0 Features

- Integrated sound controller compatible with
  - Sound Blaster Pro
  - Microsoft Windows Sound System
  - Ad Lib™ compatible
- Integrated OPTiFM™ music synthesizer with 22 voice, 52 operator synthesis, OPL3 backward compatible
- Microsoft Plug and Play compatible, supports six logical devices:
  - Sound Blaster Pro, Windows Sound System, OPL3
  - MPU-401 MIDI interface
  - IDE CD-ROM interface
  - Joystick/game port
  - Modem interface
  - 92C925 master control
- ADPCM decompression
- 8 or 16-bit sound data
  - Sound Blaster 8-bit audio up to 44.1KHz stereo
  - Windows 8/16-bit audio up to 48KHz stereo
- Integrated MIDI UART, 8-byte FIFO for both in and out with MPU-401 interface
- Built-in joystick/game port
- 18mA drivers for direct AT bus driving capabilities without additional buffers
- Power-down mode for low-power notebook applications
- OPL4 and Wave Blaster upgrade for wave table synthesis
- IDE CD-ROM drive interface
- All I/O port, IRQ and DMA are software programmable
- Silence mode to turn off all audio functions
- Volume control push-button interface
- Supports external serial EEPROM to allow easy OEM customization
- External modem chip set interface
- 100 pin package

2.1 Applications

Together with a 16-bit Codec, such as Crystal Semiconductor 4231 or Analog Devices 1845, and a serial DAC, such as Yamaha YAC512 or NEC MPD6376, the 82C925 provides an integrated solution for the following applications:

- 16-bit sound quality Sound Blaster and Windows Sound System compatible card
- Internet Phone
- 22 voice FM synthesis
- 16-bit CD-quality WAVE audio up to 48KHz stereo
- IDE CD ROM interface
- Game port
- MPU-401 and Sound Blaster MIDI interface
- OPL4 or other wave table synthesis upgrade

2.2 ISA Plug and Play on 82C925

The OPTi 82C925 supports the ISA Plug and Play (PnP) Specification 1.0a from Intel and Microsoft. After power-up, the 82C925 is isolated from other PnP cards in the host system by the system software. With this mechanism, the I/O address, IRQ and DMA usage of the 82C925 can be configured by the system according to the free resources available. As a result, the chance of getting a resource conflict is minimized.

The PnP function is enabled by default. Pull pin 55 (SPA1) of the 82C925 to low at power-up to disable PnP.

A PnP configuration sequence is carried out by either the system BIOS supporting PnP or Configuration Manager software of the operating system. It is used to map the various functional blocks (logical devices) within the 82C925 into the host system address space as well as to configure the DMA and IRQ channels. The configuration sequence occurs as follows:

1. The 82C925 is isolated from the system
2. A unique identifier (handle) is programmed into the 82C925 and the resource data is read.
3. After the resource requirement and capabilities are determined, the handle is used to assign conflict-free resources. This is done by programming the appropriate information into the 82C925 configuration registers, a logical device at a time.
4. After the configuration registers are programmed, the 82C925 leaves the configuration mode and each logical device is activated individually. The bus interface of each logical device is then enabled.

The 82C925 supports the following logical devices:

- Audio devices: including Sound Blaster Pro, Windows Sound System, and FM synthesis
- Game Port
- MPU-401 MIDI interface
- IDE CD-ROM interface
- Modem interface
- 82C925 Master Control

2.3 OPTiFM Synthesis

OPTiFM is the latest FM synthesis technology from OPTi that is included in the 82C925. OPTiFM (US patent pending) is not only backward compatible to the OPL3 standard, but is also enhanced to provide superior sound quality. Its unique modulation technique produces richer instrument sound, especially in percussion instruments. OPTiFM provides a more robust, crisp bass than that found in existing FM synthesis technology. In addition, OPTiFM also provides a very flexible way to assign operators and voices. This ensures complete backward compatibility and reserves plenty of room for handling future application requirements.

2.4 Modem Interface

The 82C925 includes the modem as a PnP logical device, as well as interface pins to connect to a modem chipset. When PnP is activated, the 82C925 provides the resource configuration for the modem chipset, such as the I/O address range and interrupt level.

The modem interface pins include pin 38 (MCS#), pin 39 (MINT), pin 32 (IRQ3) and pin 33 (IRQ4). If a modem is connected with the 82C925, the joystick port will provide support for only one joystick.

2.5 Push Button Volume Control

Two of the pins of the joystick interface can be used as volume control push-buttons (pin 36 as volume down, and pin 37 as volume up) so that the speaker volume can be controlled through front panel buttons in desktop or notebook PCs. Appropriate software drivers are needed to enable this feature.

When the volume control feature is enabled, only one joystick will be supported by the joystick port.

2.6 External Serial EEPROM

The OPTi 82C925 has the resource data and serial identifier required by the PnP specification stored internally. If the OEM customer wants to use a different resource data and serial identifier to customize their application, an external EEPROM can be used. To use an external EEPROM, pin 35 has to be pulled low. Then the resource data and serial identifier will be read from the external EEPROM instead of the 82C925 internal storage.

The OPTi 82C925 provides a serial EEPROM interface that is compatible with devices from a number of vendors. A 512-byte EEPROM is sufficient for information required by PnP. Pin 82 of the 82C925 provides the data clock for the EEPROM. Pin 83 provides data to the EEPROM, while pin 85 gets input from the EEPROM.

3.0 Signal Description

Figure 3-1 Pin Diagram

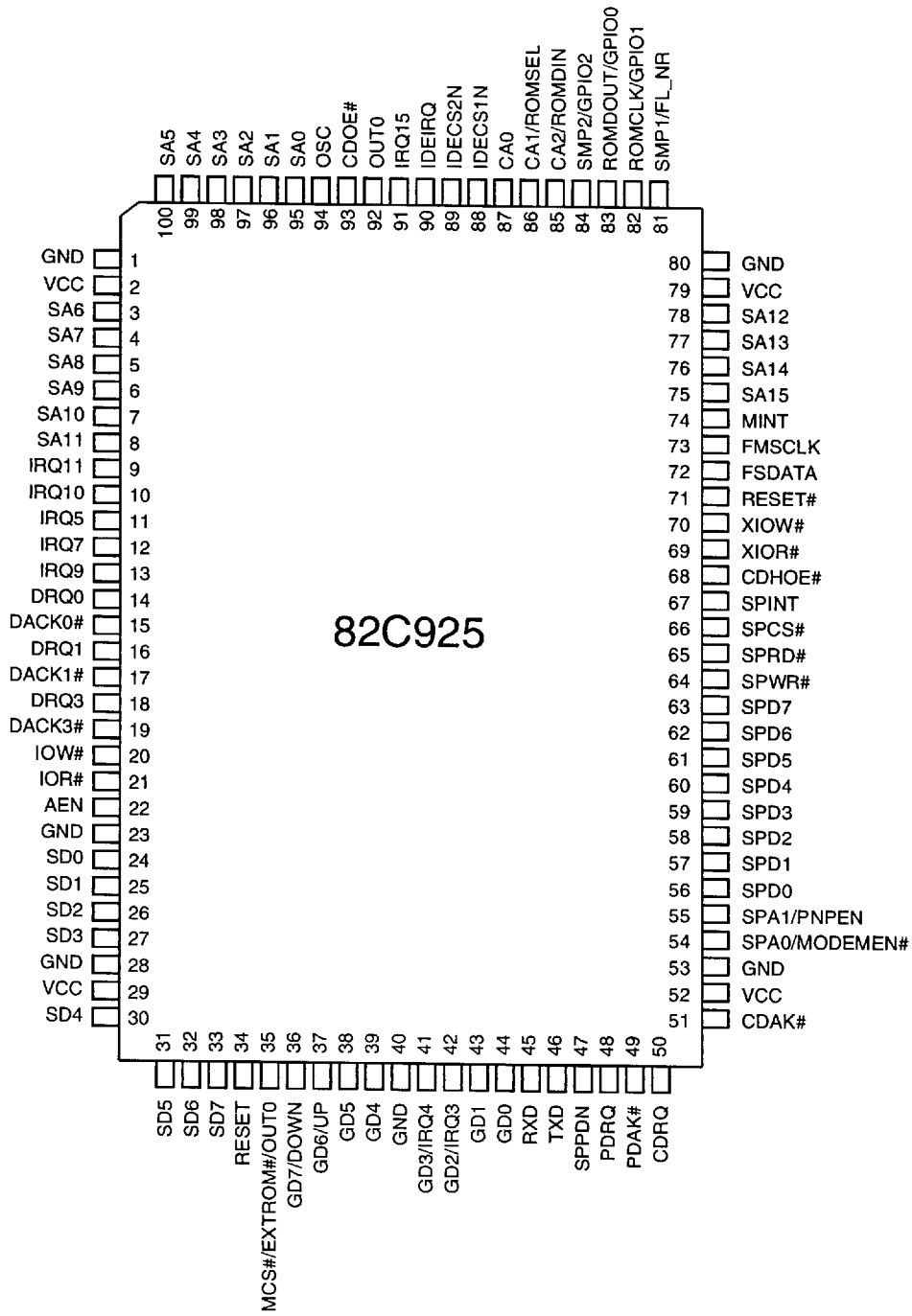


Table 3-1 Numerical Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	26	SD2	51	CDAK#	76	SA14
2	VCC	27	SD3	52	VCC	77	SA13
3	SA6	28	GND	53	GND	78	SA12
4	SA7	29	VCC	54	SPA0/MODEMEN#	79	VCC
5	SA8	30	SD4	55	SPA1/PNPEN	80	GND
6	SA9	31	SD5	56	SPD0	81	SMP1/FL_NR
7	SA10	32	SD6	57	SPD1	82	ROMCLK/GPIO1
8	SA11	33	SD7	58	SPD2	83	ROMDOUT/GPIO0
9	IRQ11	34	RESET	59	SPD3	84	SMP2/GPIO2
10	IRQ10	35	MCS#/EXTROM#/ OUT0	60	SPD4	85	CA2/ROMDIN
11	IRQ5	36	GD7/DOWN	61	SPD5	86	CA1/ROMSEL
12	IRQ7	37	GD6/UP	62	SPD6	87	CA0
13	IRQ9	38	GD5	63	SPD7	88	IDECS1N
14	DRQ0	39	GD4	64	SPWR#	89	IDECS2N
15	DACK0#	40	GND	65	SPRD#	90	IDEIRQ
16	DRQ1	41	GD3/IRQ4	66	SPCS#	91	IRQ15
17	DACK1#	42	GD2/IRQ3	67	SPINT	92	OUT0
18	DRQ3	43	GD1	68	CDHOE#	93	CDOE#
19	DACK3#	44	GD0	69	XIOR#	94	OSC
20	IOW#	45	RXD	70	XIOW#	95	SA0
21	IOR#	46	TXD	71	RESET#	96	SA1
22	AEN	47	SPPDN	72	FSDATA	97	SA2
23	GND	48	PDRQ	73	FMSCLK	98	SA3
24	SD0	49	PDAK#	74	MINT	99	SA4
25	SD1	50	CDRQ	75	SA15	100	SA5

Table 3-2 Alphabetical Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
22	AEN	23	GND	83	ROMDOUT/GPIO0	33	SD7
87	CA0	28	GND	45	RXD	81	SMP1/FL_NR
86	CA1/ROMSEL	40	GND	95	SA0	84	SMP2/GPIO2
85	CA2/ROMDIN	53	GND	96	SA1	54	SPA0/MODEMEN#
51	CDAK#	80	GND	97	SA2	55	SPA1/PNPEN
68	CDHOE#	88	IDECS1N	98	SA3	66	SPCS#
93	CDOE#	89	IDECS2N	99	SA4	56	SPD0
50	CDRQ	90	IDEIRQ	100	SA5	57	SPD1
15	DACK0#	91	IRQ15	3	SA6	58	SPD2
17	DACK1#	21	IOR#	4	SA7	59	SPD3
19	DACK3#	20	IOW#	5	SA8	60	SPD4
14	DRQ0	11	IRQ5	6	SA9	61	SPD5
16	DRQ1	12	IRQ7	7	SA10	62	SPD6
18	DRQ3	13	IRQ9	8	SA11	63	SPD7
73	FMSCLK	10	IRQ10	78	SA12	67	SPINT
72	FSDATA	9	IRQ11	77	SA13	47	SPPDN
44	GD0	35	MCS#/EXTROM#/ OUT1	76	SA14	65	SPRD#
43	GD1	74	MINT	75	SA15	64	SPWR#
42	GD2/IRQ3	94	OSC	24	SD0	46	TXD
41	GD3/IRQ4	92	OUT0	25	SD1	2	VCC
39	GD4	49	PDAK#	26	SD2	29	VCC
38	GD5	48	PDRQ	27	SD3	52	VCC
37	GD6/UP	34	RESET	30	SD4	79	VCC
36	GD7/DOWN	71	RESET#	31	SD5	69	XIOR#
1	GND	82	ROMCLK/GPIO1	32	SD6	70	XIOW#

3.1 Signal Definition

I = Input
O = Output
I/O = Bi-Directional
T = Tri-State
OD = Open-Drain

3.1.1 AT Bus Signal (41)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
IOW#	20	I	TTL-Smt 50KΩ pull-up	IO Write Command	AT BUS
IOR#	21	I	TTL-Smt 50KΩ pull-up	IO Read Command	AT BUS
AEN	22	I	TTL-Smt	DMA Address Enable	AT BUS
RESET	34	I	TTL-Smt 50KΩ pull-down	System Reset Input	AT BUS
OSC	94	I	TTL	AT 14.318MHz Clock	AT BUS
SA[15:0]	75-78,8-3, 100-95	I	TTL	System Address	AT BUS
SD[7:0]	33-30, 27-24	I/O	TTL/24mA	System Data Bus	AT BUS
DACK0# DACK1# DACK3#	15 17 19	I	TTL 50KΩ pull-up	DMA Acknowledge	AT BUS
DRQ0 DRQ1 DRQ3	14 16 18	T	18mA 50KΩ pull-down	8-Bit DMA Request	AT BUS
IRQ5 IRQ7 IRQ9 IRQ10 IRQ11 IRQ15	11 12 13 10 9 91	OD I/O OD	18mA 5KΩ pull-up TTL	Interrupt Request IRQ7-11 bidirectional for WSS auto interrupt determination IDE CD ROM Interrupt Request	AT BUS

3.1.2 MIDI Interface Signal (2)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
RXD	45	I	TTL-Smt	Receive Data	MIDI Port
TXD	46	O	18mA	Transmit Data	MIDI Port

3.1.3 FM Serial DAC Interface Signal (4)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
FMSCLK	73	O	4mA	FM Serial DAC Clock Output. This clock is used to latch serial data.	FMSDAC
FSDATA	72	O	4mA	FM Serial Data	FMSDAC

3.1.3 FM Serial DAC Interface Signal (4) (cont.)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
SMP1/FL_NR	81	I/O	TTL/4mA	Left channel sample/hold FM Serial DAC left/right clock.	FMSDAC
SMP2/GPIO2	84	I/O	TTL/4mA	Right channel sample/hold General Purpose I/O 2	FMSDAC

3.1.4 CD ROM Interface Signal (11)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
CA1/ ROMSEL	86	I/O	12mA	CD ROM Address 1 Ext. Serial EEPROM Chip Select	CD ROM PNP
CA0	87	O	12mA	CD ROM Address 0	CD RO
IDECS1N	88	O	12mA	CD ROM Chip Select	CD ROM
IDECS2N	89	I/O	TTL/12mA	CD ROM Chip Select	CD ROM
IDEIRQ	90	I	TTL/50kΩ pull-up	IDE CD ROM Interrupt Request	CD ROM
CA2/ ROMDIN	85	I/O I	TTL 12mA	CD ROM Address 2 Ext. Serial EEPROM Data In	CD ROM PNP
CDOE#	93	O	4mA	CD data buffer output enable	CD ROM
CDHOE#	68	O	4mA	CD[15:8] data buffer output enable	CD ROM
XIOR#	69	O	16mA	Buffered IOR#	CD ROM
XIOW#	70	O	12mA	Buffered IOW#	CD ROM
RESET#	71	O	12mA	Buffered RESET, active low	CD ROM

3.1.5 Game Interface Signal (8)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
GD7/DOWN GD6/UP	36 37	I I	TTL, Schmitt, pull-up TTL	Game Port Data/Volume Control	
GD5 GD4	38 39	I I	TTL TTL		
GD3/IRQ4 GD2/IRQ3	41 42	I/O I/O	16mA CMOS Schmitt	Game Port Data/Interrupt Request 4 or 3 for modem interface	
GD1 GD0	43 44	I/O I/O	TTL TTL		

3.1.6 Codec/Mixer Signal (19)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
SPA1/ PNPEN	55	I/O	TTL/4mA 50KΩ pull-up	Codec Address A0/ External PNP Enable	
SPA0/ MODEMEN#	54	I/O	TTL/4mA 50KΩ pull-up	Codec Address A0/ Modem Enable	
SPD7-SPD0	63-56	I/O	TTL/4mA 50KΩ pull-up	Codec Data	CODEC
SPWR#	64	O	4mA	Codec Write Command	CODEC
SPRD#	65	O	4mA	Codec Read Command	CODEC
SPCS#	66	O	4mA	Codec Chip Select	CODEC
SPINT	67	I	TTL	Codec Interrupt Request	CODEC
PDRQ	48	I	TTL	Playback DMA Request	CODEC
CDRQ	50	I	TTL	Capture DMA Request	CODEC
SPPDN	47	O	4mA	Codec Power-down, active low	CODEC
PDAK#	49	O	4mA	Playback DMA Acknowledge	CODEC
CDAK#	51	O	4mA	Capture DMA Acknowledge	CODEC

3.1.7 Miscellaneous (5)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
OUT0	92	O	12mA	General Purpose Output 0	
MCS#/ EXTROM#/ OUT1	35	I/O	4mA	Modem Clock/ External ROM Select#/ General Purpose Output 1	
MINT	74	I	TTL	Modem Interrupt	
ROMCLOCK/ GPIO1	82	I/O	TTL/4mA	Ext. Serial EEPROM Clock General Purpose I/O 1	
ROMDOUT/ GPIO0	83	I/O	TTL	Ext. serial EEPROM data out/ General purpose I/O 0	

3.1.8 Power Pins (10)

Pin Name	Pin #
VCC	2, 29, 52, 79
GND	1, 23, 28, 40, 53, 80

4.0 Register Description

Table 4-1 Register Map

I/O Address	Description	R/W
SBBase + 0 ALBase + 0	Left FM Status Port	R only
SBBase + 0 ALBase + 0	Left FM Register Address Port	W only
SBBase + 1 ALBase + 1	Left FM Data Port	W only
SBBase + 2 ALBase + 2	Right FM Register Address Port	W only
SBBase + 3 ALBase + 3	Right FM Data Port	W only
SBBase + 4	Mixer Address Port	W only
SBBase + 5	Mixer Data Port	R/W
SBBase + 6	Digital Audio Processor Software Reset	W only
SBBase + 8	FM Status Port	R only
SBBase + 8	FM Register Address Port	W only
SBBase + 9	FM Data Port	W only
SBBase + A	Digital Audio Processor Read Data	R only, Digital Audio Processor AO = 0
SBBase + C	Digital Audio Processor Write Data/ Cmd	W only, Digital Audio Processor AO = 1
SBBase + C	Digital Audio Processor Write Buffer Status	R only, Digital Audio Processor AO = 1
SBBase + E	Digital Audio Processor Output Buffer Status Register	R only, Digital Audio Processor AO = 1
WSBase + 0-3	Configuration	W only
WSBase + 0-3	Version	R only
WSBase + 4	Codec Index Register	R/W, exists in Codec and shadowed in 82C925
WSBase + 5	Codec Indexed Data Register	R/W, exists in Codec only
WSBase + 6	Codec Status Register	R/W, exists in Codec only
WSBase + 7	Codec Direct Data	R/W, exists in Codec only
200-207	Game Port	R/W
CDBase + 0-3	CD ROM Interface Registers	R/W
MCBase + 3 ($F8F)	Password Register	W only
MCBase + 1 ($F8D)	MC1	R/W
MCBase + 2 ($F8E)	MC2	R/W
MCBase + 3 ($F8F)	MC3	R/W

Table 4-1 Register Map (cont.)

I/O Address	Description	R/W
MCBase + 4 ($F90)	MC4	R/W
MCBase + 5 ($F91)	MC5	R/W
MCBase + 6 ($F92)	MC6	R/W
MCBase + 7 ($F93)	MC7	R/W
MCBase + 8 ($F94)	MC Indirect Index	R/W
MCBase + 9 ($F95)	MC Indirect Data	R/W
279	PNP Address	W
A79	PNP Write_Data	W
PNPBase	PNP Read_Data	R

4.1 Register Definition

Mode Control Register 1
Note: Password = "E5".

MC1(F8D) R/W with password, MC1[3:0] jumper initialized							
7	6	5	4	3	2	1	0
MOD	PDN	Sound Base[1:0]		CDTYPE[2:0]			GPEN#

MOD: Operation Mode
0 = Sound Blaster compatible mode (default)
1 = Windows Sound System compatible

PDN: Power-down Mode
0 = Normal (default)
1 = Power-down: all internal clocks are stopped and FMCLK is stopped in high level

Sound Base: I/O Base Address
In Windows Sound System mode, MC[5:4] select the I/O base address among four specified addresses
00:WSBase = 530 (default)
01: WSBase = E80
10: WSBase = F40
11: WSBase = 604

CD Type: Type of CD ROM interface
000: CD Disabled (default)
001: Reserved
010: Reserved
011: Reserved
100: Secondary IDE
101: Reserved
110: Reserved
111: Chip Test Mode

GPEN#: Game Port Enable
0: Enable (default)
1: Disable

Default = 00h

Mode Control Register 2

MC2 (F8E) R/W with password							
7	6	5	4	3	2	1	0
RESERVED		OPL4	RESERVED			RESERVED	

OPL4: Yamaha OPL4 Synthesis Chip
0 = OPL3 FM synthesis chip is assumed (default)
1 = OPL4 Wave Table synthesis chip is assumed

Default = 03h

Mode Control Register 3

MC3 (F8F) R/W with password							
7	6	5	4	3	2	1	0
DAIRQ[1:0]		DADRQ[1:0]		Reserved	DABASE	REV[1]/ WRSROM	Reserved

DAIRQ: Digital Audio Interrupt Request Select for Sound Blaster Mode
00: IRQ = 7
01: IRQ = 10
10: IRQ = 5
11: IRQ = disabled

DADRQ: Digital Audio DMA Channel Select for Sound Blaster Mode
00: DRQ = 1
01: DRQ = 0
10: DRQ = 3
11: DRQ = disabled

DABASE: DA Base Address
0 = 220h
1 =240h

REV[1]/WRSROM:
Read: Chip ID high bit
Write: Enable write to external EPROM

Default = F2h

Mode Control Register 4

MC4 (F90)							
7	6	5	4	3	2	1	0
Reserved	OUT0	Reserved	PNP MODE#	FMCLK	SILENCE	SBVER	

OUT0: General Purpose Output 0

PNP MODE#: Reserved
0 = PNP Mode
1 = 929 mode for older game compatibility

FMCLK: OPLx Clock Output Enable
0 = OPL3
1 = OPL2

SILENCE: Audio Interface Enable
0 = Enabled
1 = Disabled

SBVER: Sound Blaster Version
00: Version 2.1
01: Version 1.5
10: Version 3.2
11: Version 4.4

Default = A2h

Mode Control Register 5 - Diagnostic Register

MC5 (F91)							
7	6	5	4	3	2	1	0
AVCEN#	OPL5	Reserved					

AVCEN#: Automatic Volume Control, active low
0 = Enable
1 = Disable

OPL5: OPL5 Address Decoding, reserved
1 = Select the OPL5 address decoding

Default = 2F

Mode Control Register 6 - MIDI Interface

MC6 (F92) Write Only							
7	6	5	4	3	2	1	0
MPU-401	MPU-401 BA		MPU-401 INT		Reserved		

MPU-401: Select MPU-401
0 = Disable
1 = Enable

MPU-401 BA: MPU-401 Base Address Select
00 = 330h
01 = 320h
10 = 310h
11 = 300h

MPU-401 INT: MPU-401 Interrupt Select
00 = IRQ9
01 = IRQ10
10 = IRQ5
11 = IRQ7

Default = 83h

Mode Control Register 7 - Volume Control

MC7 (F93)							
7	6	5	4	3	2	1	0
VCINT EN	PNP TEST	MC MUTE	ATTN4	ATTN3	ATTN2	ATTN1	ATTN0

VCINT EN: Volume Control Interrupt Enable
PNP TEST: PNP Test Mode
MC MUTE: Mute WAVE Output
ATTN[4:0]: WAVE Volume Adjustment
When WRSROM (MC3[1]) is active, ATTN [2:0] are used to write to external EPROM, as follows:
ATTN0 = ROMDOUT, ATTN1 = SROMCLK, ATTN2 = SROMCS

Mode Control Register 8

MC8 (indirect)							
7	6	5	4	3	2	1	0
MECRDY	MECEMP	MECINT	MECISEL[1:0]		RESERVED		EXTROM#

MC8[7:5]: Reserved
MECISEL[1:0]: Volume Control Interrupt Select
00 = Disabled
01 = IRQ5
10 = IRQ10
11 = IRQ11
MC8[2:1]: Reserved
EXTROM#: External ROM select setting status
0 = Enabled
1 = Disabled

Mode Control Register 9

MC9 (indirect) Read Only							
7	6	5	4	3	2	1	0
CSNN	MODEMEN	MODEMIO1	MODEMIO0	CONFIG	ISOLATION	SLEEP	WAIT KEY

MC9[7:0]: Reserved

Mode Control Register 10

MC10 (indirect) Read Only							
7	6	5	4	3	2	1	0
RESEVED							

Mode Control Register 11

MC11 (indirect) Read Only							
7	6	5	4	3	2	1	0
RESERVED							

Mode Control Register 12

MC12 (indirect) Read Only							
7	6	5	4	3	2	1	0
IDEEN	BUTUP	BUTDN	BUTMUTE	BUTINT	PNPEN	Reserved	

IDEEN: IDE CD-ROM device enabled
BUTUP: Volume up button pushed
BUTDN: Volume down button pushed
BUTMUTE: Both up and down buttons pushed
BUTINT: Volume control interrupt pending
PNPEN: Plug and Play mode enabled
MC12[1:0]: Reserved

Note: Read of MC12 will clear BUTUP, BUTDN, BUTMUTE, and BUTINT.

Mode Control Register 13

MC13 (indirect) Read/Write							
7	6	5	4	3	2	1	0
RESERVED			FMTEST	MEGABASS	OPTIMODE	YFDAC	INTFM

MC13[7:5]: Reserved
FMTEST: FM test mode enable
MEGABASS: Mega Bass enable
0 = Disable
1 = Enable
OPTIMODE: OPTi Mode enable
0 = Disable (default)
1 = Enable
YFDAC: Yamaha DAC select
0 = Enable Yamaha format
1 = Disable Yamaha format, use NEC PD6376GS format
INTFM: Internal FM
0 = Internal OPTiFM (default)
1 = Use external FM

Mode Control Register 14

MC14 (indirect) Read/Write							
7	6	5	4	3	2	1	0
Reserved		GPIO2	GPIO2 CTR	GPIO1	GPIO1 CTR	GPIO0	GPIO0 CTR

GPIOx: General Purpose Register
GPIOx CTR: General Purpose Register I/O Control
0 = input
1 = output

Mode Control Index Register

MC Indirect Index (F94)							
7	6	5	4	3	2	1	0

Mode Control Indirect Data Register

MC Indirect Data (F95)							
7	6	5	4	3	2	1	0

Digital Audio Processor Register 1

DAP Reset (SBBase+B) Write Only							
7	6	5	4	3	2	1	0
Reserved							RESET

RESET: Reset
0 = System reset will reset the software reset flag and terminate software reset.

1 = Software reset on the DAP at the end of the IO write command.
It actually sets a software reset flag.

Digital Audio Processor Register 2

DAP Read Data (SBBase+A) Read Only							
7	6	5	4	3	2	1	0
DATA							

This is the data output port of the Digital Audio Processor.

Digital Audio Processor Register 3

DAP Write Buffer Status (SBBase+C) Read Format							
7	6	5	4	3	2	1	0
IBFULL	(SBBase+A)[6:0]						

IBFULL: Input Buffer Full.
0 = DAP input buffer empty.
1 = DAP Input Buffer full.
This flag is set when the host CPU writes data in the input data bus buffer and cleared when the data is read by the internal digital audio processor.

Digital Audio Processor Register 4

DAP Data/Command Register (SBBase+C) Write Format							
7	6	5	4	3	2	1	0
Command/Data							

This is the data/command write port for the Digital Audio Processor.

Digital Audio Processor Register 5

DAP Output Buffer Status (SBBase+E) Read Only							
7	6	5	4	3	2	1	0
OBFULL	Output Buffer [6:0]						

OBFULL: Output Buffer Full.
0 = DAP output buffer empty.
1 = DAP output buffer full.
This flag is set in the digital audio processor when data is written in the output data bus buffer and cleared when the host CPU or the DMA controller reads the data in the output data bus buffer.
Reading this register will also clear the Digital Audio Processor interrupt request.

Windows Sound System Configuration Register

WSBase+0-3 Write Only							
7	6	5	4	3	2	1	0
Reserved	ISS	WSIRQ			WSDRQ		

ISS: IRQ Sense Source
0 = Normal
1 = Auto-Interrupt Selection

WSIRQ: IRQ Select
000 = Disabled
001 = IRQ7
010 = IRQ9
011 = IRQ10
100 = IRQ11
101, 110, 111 = Reserved

WSDRQ: DMA Request Select

	Playback	Capture
000	Disabled	Disabled
001	DRQ0	Disabled
010	DRQ1	Disabled
011	DRQ3	Disabled
100	Disabled	DRQ1
101	DRQ0	DRQ1
110	DRQ1	DRQ0
111	DRQ3	DRQ0

Windows Sound System Version Register

WSBase+0-3 Read Only							
7	6	5	4	3	2	1	0
CHANNEL	IRQSENSE	VERSION					

CHANNEL: Channel Available
0 = DRQ0/1/3 and IRQ7/9/10/11 available
1 = DRQ1/3 and IRQ7/9 available

IRQSENSE: 0 = No interrupt
1 = WSS interrupt active

VERSION: 04h

5.0 Electrical Specification

5.1 Absolute Maximum Ratings

Sym.	Description	Min	Max	Units
VDD	Supply Voltage	-0.5	6.5	V
VI	Input Voltage	-0.5	VDD + 0.5	V
VO	Output Voltage	-0.5	VDD + 0.5	V
TSTG	Storage Temperature	-40	125	°C
	Power Dissipation	TBD	TBD	V

5.2 Recommended DC Operating Conditions

Sym.	Description	Min	Max	Units
VDD	Supply Voltage	4.5	5.5	V
AVD	Supply Voltage	4.75	5.25	V
TOP	Operating Temperature	0	70	°C

5.3 General Specification (VDD = 5.0V)

Sym.	Description	Condition	Min	Typ.	Max	Units
IIL	Low Level Input Current	VIN = VSS	-10		+10	uA
IIH	High Level Input Current	VIN = VDD	-10		+10	uA
IOZ	Tri-State Output Leakage Current	VOUT = 0/VDD	-10		+10	uA
V-	Schmitt Negative Threshold	TTL-STATIC CMOS-STATIC	0.8 1.5		1.3 2.5	V
V+	Schmitt Positive Threshold	TTL-STATIC CMOS-STATIC	1.4 2.5		2.1 3.5	V
VH	Schmitt Hysteresis	TTL-STATIC CMOS-static		0.6 1.0		V
VIL	low Level Input Voltage	TTL-STATIC			0.8	V
VIH	High Level Input Voltage	TTL-STATIC	2.0			V
VOL	Low Level Output Voltage	TTL-STATIC			0.4	V
VOH	High Level Output Voltage	TTL-STATIC	2.4			V
RPD	Pull-Down Resistance	VIN = VDD	50		200	KΩ
RPU	Pull-Up Resistance	VIN = VSS	50		200	KΩ
CIN	Input Capacitance	FREQ = 1MHz @ 0V			5	pF
COUT	Output Capacitance	FREQ = 1MHz @ 0V			5	pF
CIO	Bi-Directional Capacitance	FREQ = 1MHz @ 0V			5	pF

Sym.	Description	Condition	Min	Typ.	Max	Units
IOS	Short Circuit Output Current	VOUT = 0V		2	25	mA
IKLU	I/O Latch-Up Current	V < VSS, V > VDD	100			mA
VESD	Electrostatic Protection	C = 100PF, R = 1.5KΩ	2000			V

5.4 Timing Parameters

5.4.1 AT Bus Timing

Description	Sym	Min	Max	Units
OSC (14.318 MHz) Frequency	TOSCP	14.000	14.500	MHz
OSC High Width	TOSCH	32	40	ns
OSC Low Width	TOSCL	32	40	ns
RESET to RST#	TRST	40	80	ns
IOR#/IOW# Command Width	TCMDW	120		ns
Write Data Setup to IOW# Rising	TWDSU	30		ns
Write Data Hold from IOW# Rising	TWDHD	15		ns
Read Access Time	TRAC	20	50	ns
Address Setup to IOR#/IOW# Falling	TASU	50		ns
Address Hold from IOR#/IOW# Rising	TAHD	30		ns
DACK# Setup to IOR#/IOW# Falling	TDKSU	40		ns
DACK# Hold from IOR#/IOW# Rising	TDKHD	160		ns
SD Hold from IOR# Rising	TDHR	0	20	ns
DRQ Hold from IOR#/IOW# Falling	TDRHD	0	25	ns

5.4.2 CD ROM/FM/Game Port Interface Timing

Description	Sym	Min	Max	Units
SA to CA Delay	TCA	3	20	ns
SA to XCS#/FMCS#/MIXCS#	TXCS	5	20	ns
SD to XD Delay	TXD	5	30	ns
XD to SD Delay	TXSD	5	30	ns
XD Read Data Hold	TXDH	5		ns
IOR#/IOW# to XIOR#/XIOW# Delay IOR#/IOW# to GPR#/GPW# Delay	TCMDD	3	20	ns
IOW# to XD Enable Delay	TXDE	5	20	ns
XDRQ to DRQ# Delay	TDRQ	5	20	ns
DACK# to XDAK# Delay	TXDAK	5	20	ns

5.4.3 AD1848 Interface Timimg

Description	Sym	Min	Max	Units
SA to SPCS# Delay	TSPCS	5	20	ns
SD to SPD Delay	TSPD	5	25	ns
SPD to SD Delay	TSPSD	5	20	ns
SPD Read Data Hold	TSPDH	5		ns
IOR#/IOW# to SPR#/SPW# Delay	TSPW	3	20	ns
IOW# to SPD Enable Delay	TSPDE	5	20	ns
IOW# rising to SPD Disable Delay	TSPDN	10	40	ns
DACK# to PDAK#/CDAK# Delay	TXDAK	5	20	ns

5.5 DC Electrical Characteristics

Description	Sym	Min	Max	Units	Conditions
Operating Supply Voltage	Vcc	4.5	5.5	V	
High Level Input Voltage	VIH	2.4	Vcc + 0.3	V	VCC = min
High Level Input Voltage for RESET	VIHa	3.5	Vcc + 0.3	V	VCC = min
Low Level Input Voltage	Vil	-0.3	0.8	V	VCC = max
High Level Output Voltage	VOH	Vcc-0.5	Vcc	V	IOH = -4mA VCC = max
Low Level Output Voltage	VOL		0.2	V	IOL = 4MA VCC = min
Input Leakage Current	IIL		10	uA	VCC = max
Input Leakage Current with 5K pull-up resistor	IILa	-100	-500	uA	VIN = 0V
Input Leakage Current with 50K pull-up resistor	IILb	-10	-50	uA	VIN = 0V
Output Leakage Current	IOL		10	uA	VCC = max
Static or Power-down Mode Current	IPD		300	uA	VCC = max

5.6 Absolute Maximum Ratings

Description	Sym	Min	Max	Units	Conditions
Supply Voltage	VCC	-0.3	7.0	V	
Storage Temperature	TS	-65	+125	C	
Ambient Operating Temperature	Ta	-45	+85	C	

5.7 Timing Characteristics

Figure 5-1 Register/CD/FM/Mixer/Sound Port IO Read Cycle

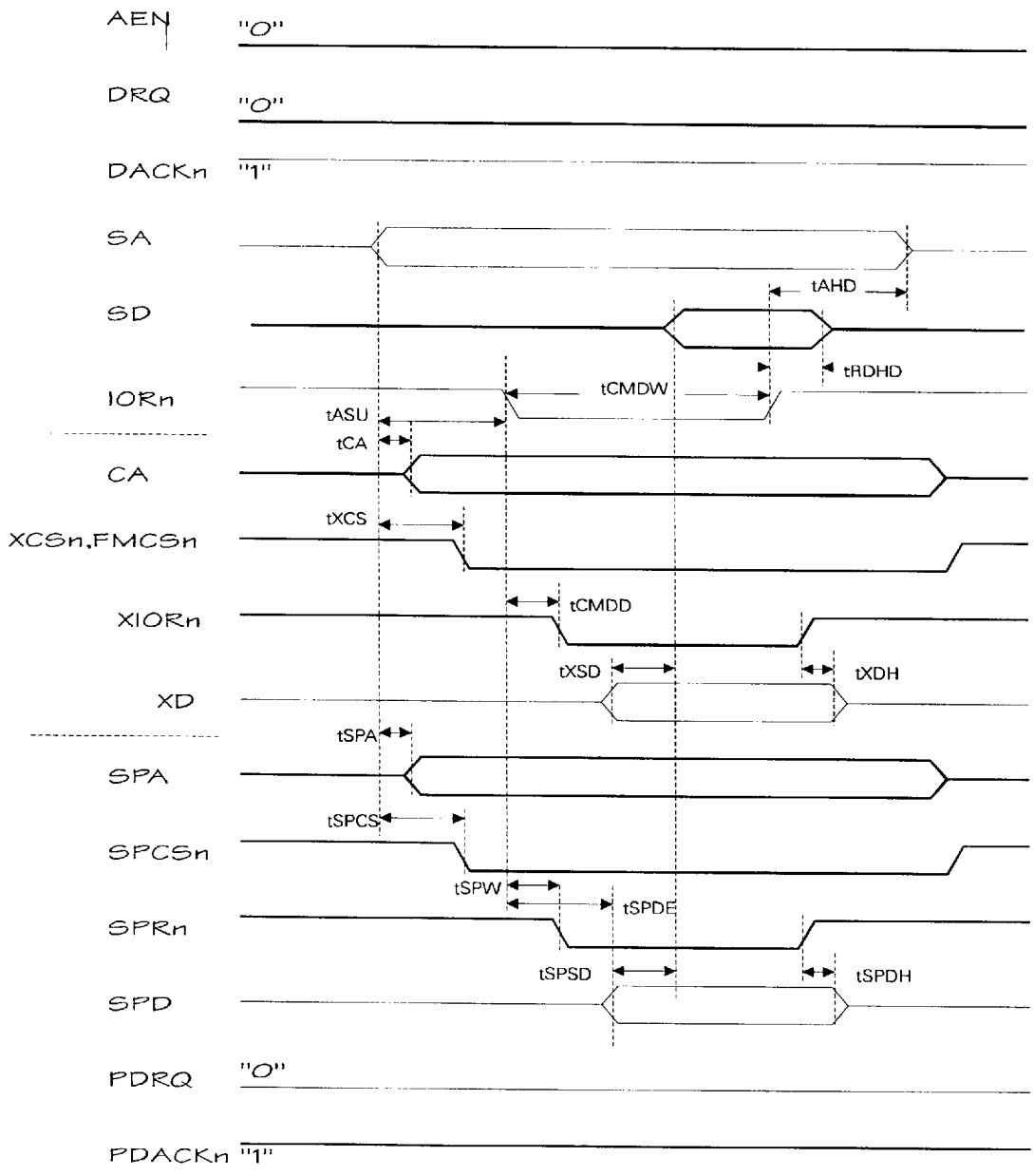


Figure 5-2 DMA Write/Playback Cycle

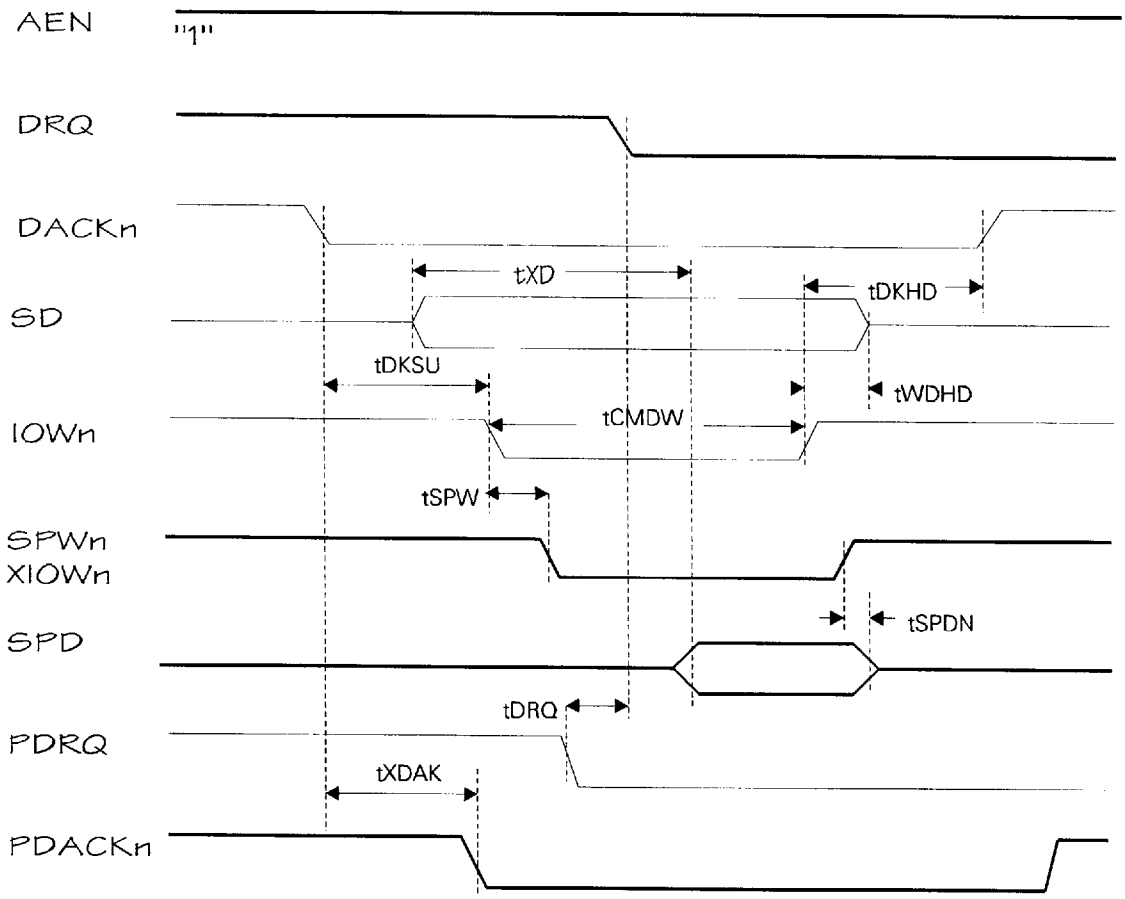


Figure 5-3 DMA Read/Capture Cycle

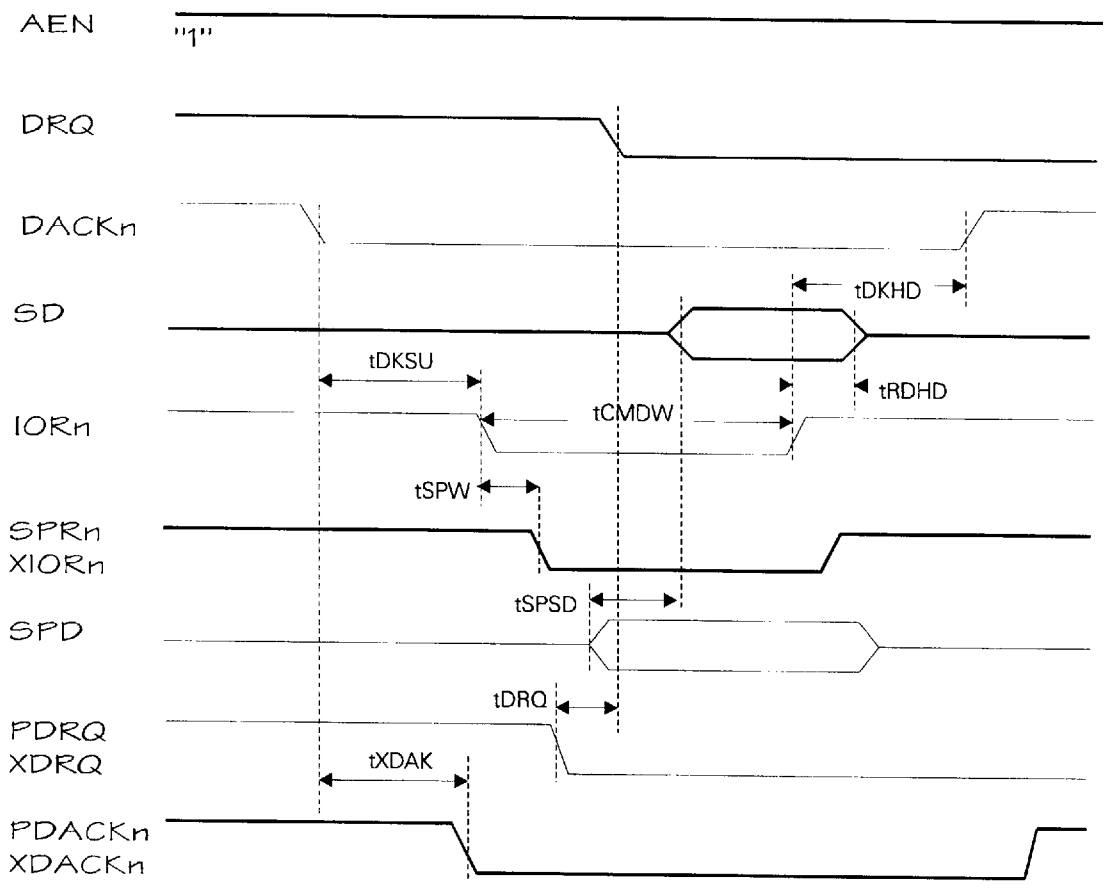
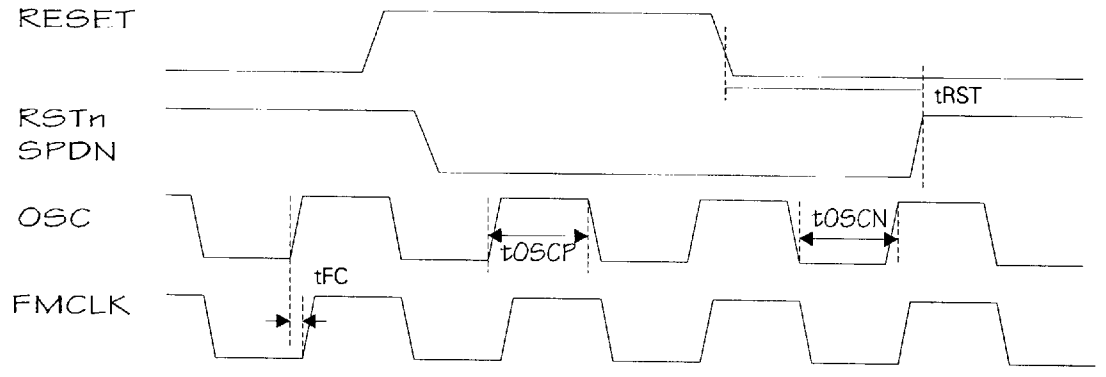
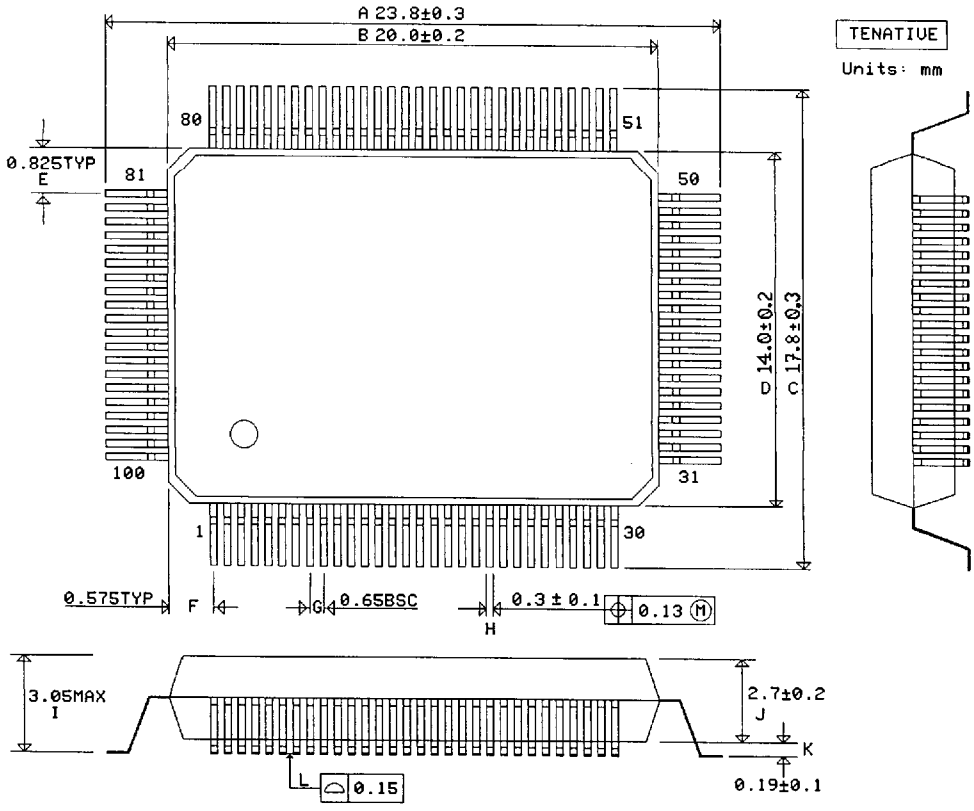


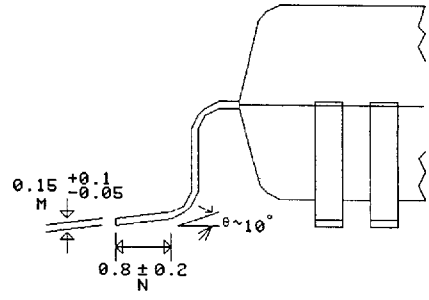
Figure 5-4 RESET and CLK Timing



6.0 Mechanical Package

Figure 6-1 Mechanical Outline Package





DIM	MILLIMETERS		INCHES		DESCRIPTION
	MIN	MAX	MIN	MAX	
A	23.5	24.1	.925"	.949"	Maximum Width LEAD TO LEAD
B	19.8	20.2	.779"	.795"	Maximum Width PACKAGE ENVELOPE
C	17.5	18.1	.689"	.713"	Maximum Height LEAD TO LEAD
D	13.8	14.2	.543"	.559"	Maximum Height PACKAGE ENVELOPE
E	0.825 TYP		.0325" TYP		LEAD CENTER TO PERP. LEAD PLANE
F	0.575 TYP		.0226" TYP		LEAD CENTER TO PERP. LEAD PLANE
G	0.65 BSC		.0256" BSC		LEAD TO LEAD CENTER SPACING
H	0.2	0.4	.008"	.016"	LEAD WIDTH
I	——	3.05	——	.120"	PACKAGE HEIGHT LEAD PLANE TO TOP
J	2.5	2.9	.098"	.114"	MAXIMUM THICKNESS PACKAGE ENVELOPE
K	0.09	0.29	.0035"	.0114"	LEAD PLANE TO PACKAGE BOTTOM
L	——	0.15	——	.006"	LEAD PLANE SKEW
M	0.1	0.25	.004"	.010"	LEAD THICKNESS
N	0.6	1.0	.024"	.039"	LEAD FOOTPRINT