OKI semiconductor

MSM65512/65P512

T-49-19-08

OKI ORIGINAL HIGH PERFORMANCE CMOS 8 BIT SINGLE CHIP MICROCONTROLLER

GENERAL DESCRIPTION

MSM65512 is a high-performance 8-bit single-chip controller that employs Oki's original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65512 is capable of high-speed processing, and includes 8 Kbytes of program memory, 256 bytes of data memory, timers and serial ports on chip. Also available is the MSM65P512, which replaces the on-chip program memory with one-time PROM.

OPERATING RANGE

- Operating Frequency : DC ~ 10 MHz
- Operating Voltage : 4.5 ~ 5.5 V
- Operating Temperature : -40 ~ 85°C

FEATURES

- Memory Space : 64 Kbytes

  On-Chip Program Memory : 8 Kbytes
  On-Chip Data Memory : 256 bytes
- Minimum Instruction Execution Cycle:
  400nS @ 10 MHz
- Powerful instruction set:

  83 basic instructions
  8/16-bit operation instructions
  Bit manipulation instructions
  Compound function instructions
- Abundant addressing modes
- Multiplication/division operation functions
  16 ← 8 x 8
  16 ← 16/8, 8 ← 16 mod 8
- I/O ports: 8-bit x 4
- Timers
  8-bit auto-reload timer x 2
  16-bit auto-reload timer x 1
  Watchdog timer x 1
- Counters
  Time base counter x 1
  16-bit free-running counter x 1
- Capture input: 1 channel
- Compare output: 2 channels
- Serial ports

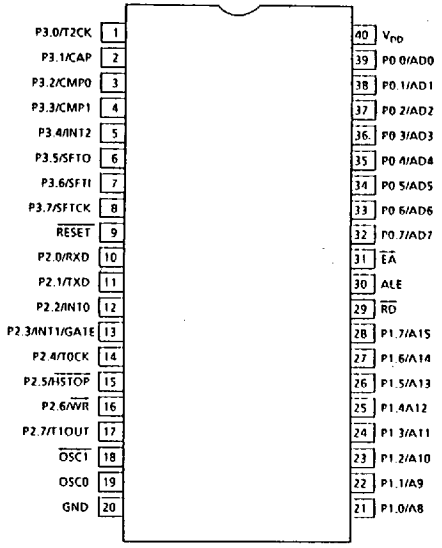
  Shift register x 1

  Serial port with baud rate generator (UART/synchronous) x 1
- External interrupts: 3
- Interrupt factors: 15
- Package:
  40 pin plastic DIP (DIP40-P-600)
  44 pin plastic QFP (QFP44-P-910-K)
  44 pin PLCC (QFJ44-P-S650)
  64 pin plastic QFP (QFP64-P-1414-1K)

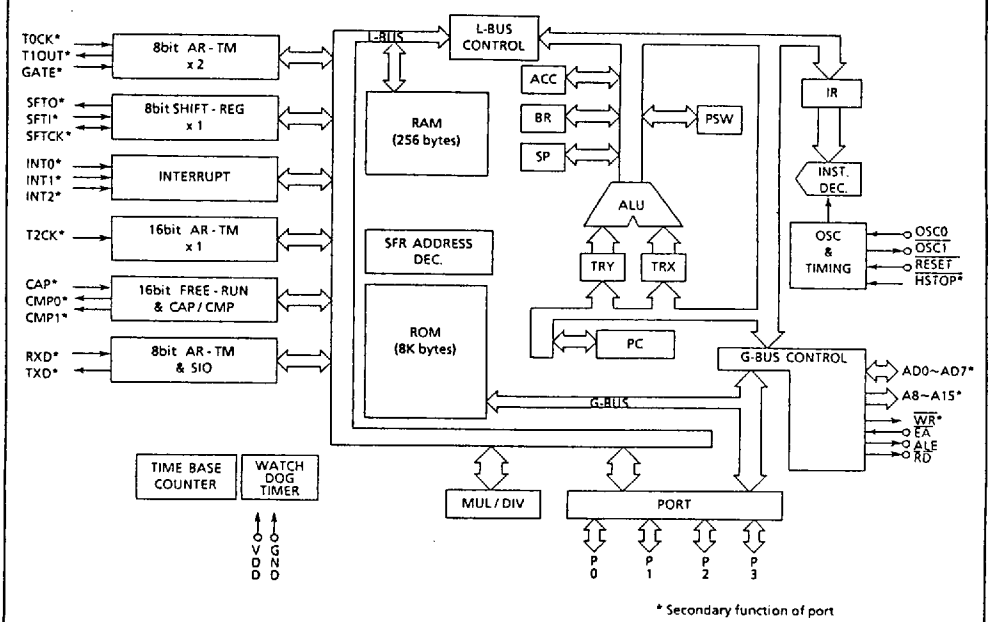
* Specifications are subject to change without notice.

PIN CONFIGURATION

40-Pin Plastic DIP
(Top View)



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

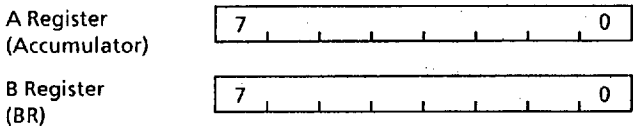
Type	Pin Name	I/O	Description
Power supply	VDD		+ 5 V power supply
	GND		0 V ground
Oscillation	OSC0	Input	System clock input pin. Quartz oscillator or ceramic oscillator is connected between OSC0 and $\overline{OSC1}$. For external clock, input at OSC0, leaving $\overline{OSC1}$ open.
	$\overline{OSC1}$	Output	System clock output pin
Control	$\overline{RESET}$	Input	System reset input (program starts from address 0040H); internal pull-up resistance
	$\overline{EA}$	Input	Program memory select input pin. "L" level input for external program memory; "H" level input for internal program memory.
	$\overline{RD}$	Output	Read strobe signal during external memory access
	ALE	Output	Address latch signal during external memory access
Port	PORT 0	I/O	8-bit I/O port During external memory access, becomes address/data bus for address output, instruction fetch or data read/write along with ALE, $\overline{RD}$ and $\overline{WR}$ pins
	PORT 1	I/O	8-bit I/O port Address bus during external memory access
	PORT 2 PORT 3	I/O	8-bit I/O port x 2. Secondary functions shown in following table are added for ports 2 and 3.

PIN SECONDARY FUNCTIONS

Pin Name	I/O	Description
RXD	I/O	P2.0 secondary functions. UART: Input pin for serial port receive data. Synchronous: Input pin for serial port transmit/receive data.
TXD	Output	P2.1 secondary functions. UART: Output pin for serial port transmit data. Synchronous: Output pin for serial port synchronizing clock.
INT0	Input	P2.2 secondary function. External interrupt 0 input pin.
INT1/GATE	Input	P2.3 secondary functions. External interrupt 1 input pin. Also used as input pin for gate signal for timer 0 count enable /disable.
T0CK	Input	P2.4 secondary function Timer 0 external clock input pin.
$\overline{\text{HSTOP}}$	Input	P2.5 secondary function. Hard stop mode input pin; stops system clock oscillation with "L" level input.
$\overline{\text{WR}}$	Output	P2.6 secondary function. Write strobe signal output pin during external data memory access.
T1OUT	Output	P2.7 secondary function. Output pin for signal that 2-divided timer 1 overflow.
T2CK	Input	P3.0 secondary function. Timer 2 external clock input pin.
CAP	Input	P3.1 secondary function. Capture trigger input pin.
CMP0	Output	P3.2 secondary function. Compare output channel 0 output pin.
CMP1	Output	P3.3 secondary function. Compare output channel 1 output pin.
INT2	Input	P3.4 secondary function. External interrupt 2 input signal.
SFTO	Output	P3.5 secondary function. Shift register data output pin.
SFTI	Input	P3.6 secondary function. Shift register data input signal.
SFTCK	I/O	P3.7 secondary function. Shift register synchronizing clock input/output signal.

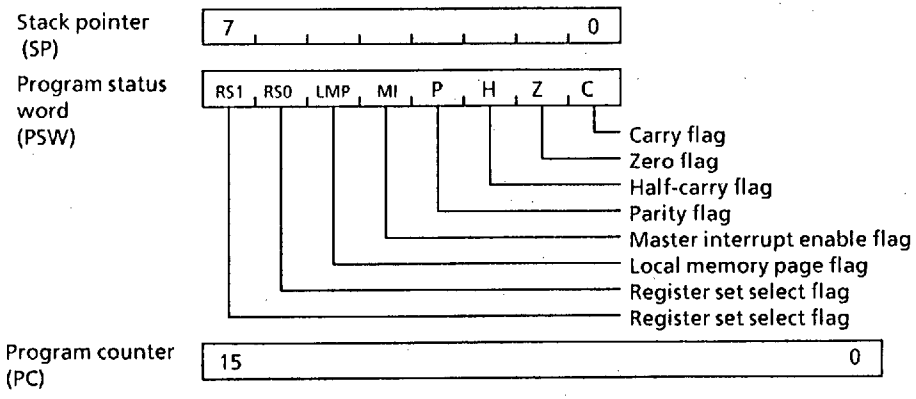
REGISTERS

• Operation Registers

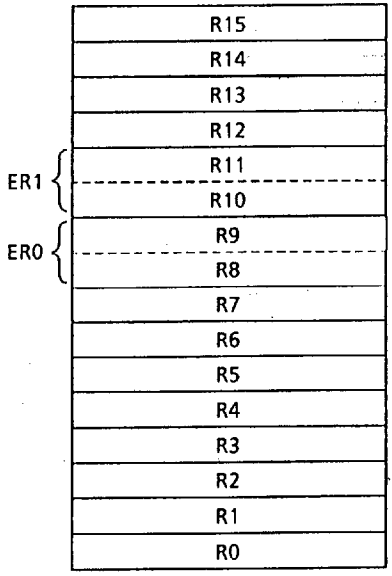


* For 16-bit operation instruction, A register holds low byte data and the B register holds high byte data.

• Special Purpose Registers



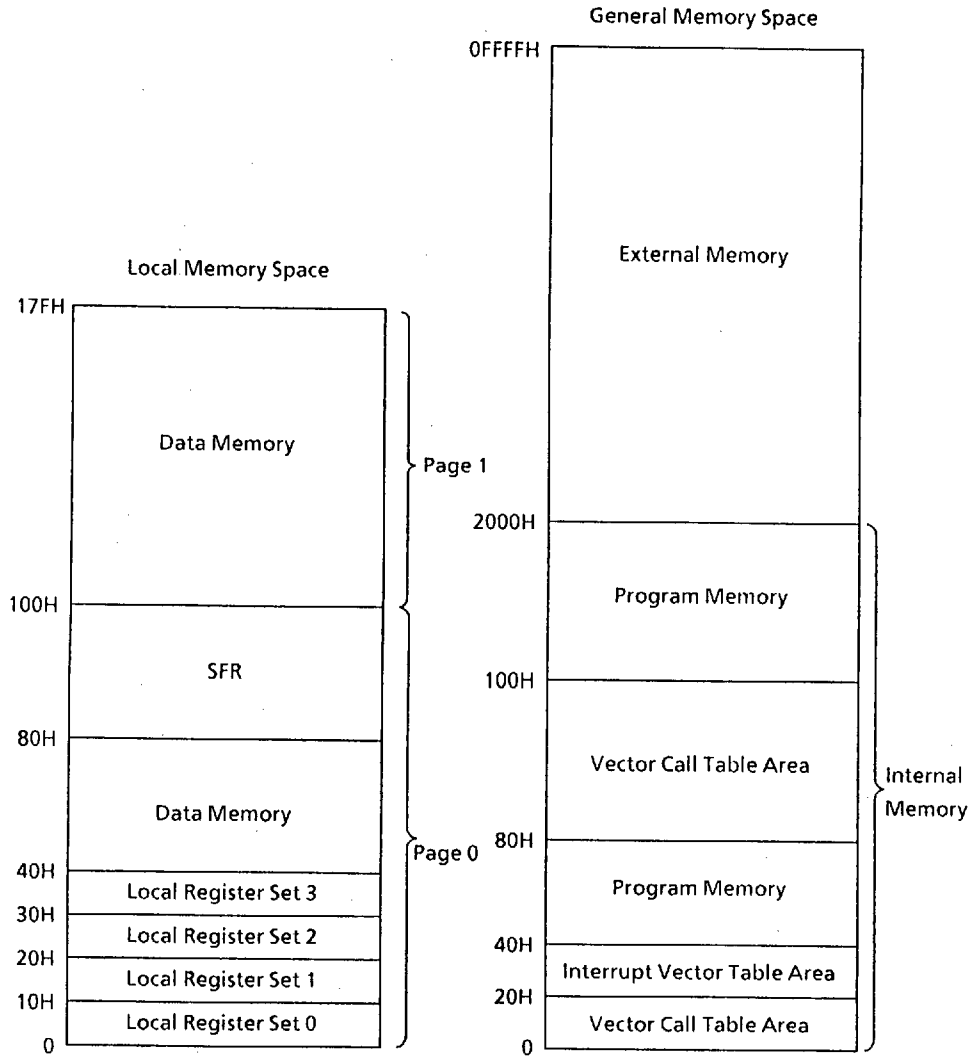
LOCAL REGISTERS



*1 4 banks of local registers are mapped in local memory space data memory.

*2 Registers R8 to R11 can be used as 16-bit registers, ER0 and ER1.

MEMORY MAPS


General Memory Space
0FFFFH
External Memory
2000H
Program Memory
100H
Vector Call Table Area
80H
Program Memory
40H
Interrupt Vector Table Area
20H
Vector Call Table Area
0
Internal Memory
Local Memory Space
17FH
Data Memory
Page 1
100H
SFR
80H
Data Memory
Page 0
40H
Local Register Set 3
30H
Local Register Set 2
20H
Local Register Set 1
10H
Local Register Set 0
0

SFR TABLE

Address (HEX)	Name	Sym-bol	Symbol	R/W	Reset
0FF	F register (multiplication/division operation register)	FER	FR	R/W	00H
0FE	E register (multiplication/division operation register)		ER		00H
0FD	D register (multiplication/division operation register)	DCR	DR		00H
0FC	C register (multiplication/division operation register)		CR		00H
0FB	Multiplication/division condition register		MDCR		0FCH
0F7	Interrupt enable register	IE	IEH	R/W	70H
0F6			IEL		00H
0F5	Interrupt request register	IRQ	IRQH		70H
0F4			IRQL		00H
0F3	External interrupt control register		XICON		0C0H
0F2	Standby control register		SBYCON		0F0H
0F1	Stack page specification register		SPR		0FEH
0F0	Watchdog timer control register		WDTCON	W	—
0EE	Port 3 mode register		P3MOD	R/W	53H
0ED	Port 3 direction register		P3DIR		00H
0EC	Port 3 data register		P3D		Unde-fined
0EA	Port 2 mode register		P2MOD		3CH
0E9	Port 2 direction register		P2DIR		00H
0E8	Port 2 data register		P2D		Unde-fined
0E5	Port 1 direction register		P1DIR		00H
0E4	Port 1 data register		P1D		Unde-fined
0E3	Port 0 direction register		P0DIR		00H
0E2	Port 0 data register		P0D		Unde-fined
0E1	Shift register		SFTR		Unde-fined
0E0	Shift register control register		SFTCON		0E0H

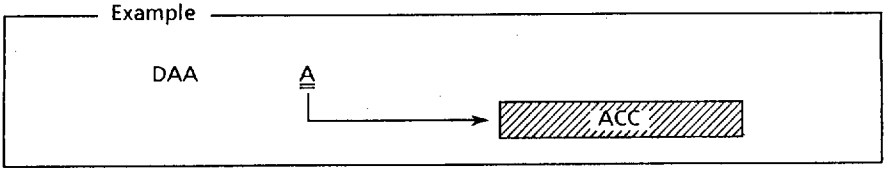
Address (HEX)	Name	Symbol	Symbol	R/W	Reset
0DF	Timer 1 register	T01R	T1R	R/W	Undefined
0DE	Timer 0 register		T0R		Undefined
0DD	Timer 1 counter	T01C	T1C		Undefined
0DC	Timer 0 counter		T0C		Undefined
0DB	Timer 1 control register		T1CON		0F0H
0DA	Timer 0 control register		T0CON		0E0H
0D9	Time base counter control register		TBCON		0E0H
0D7	Timer 2 register	T2R	T2RH		Undefined
0D6			T2RL		Undefined
0D5	Timer 2 counter	T2C	T2CH		Undefined
0D4			T2CL		Undefined
0D3	Timer 2 control register		T2CON		0F4H
0D2	Free-running counter	FRC	FRCH		00H
0D1			FRCL		00H
0D0	Free-running counter control register		FRCON		0F4H
0CF	Compare channel 1 data register	CMP1R	CMP1RH		Undefined
0CE			CMP1RL		Undefined
0CD	Compare channel 0 data register	CMP0R	CMP0RH		Undefined
0CC			CMP0RL		Undefined
0CB	Compare output control register		CMPCON		0F0H
0CA	Compare output data register		CMPOUT		0FCH
0C9	Capture data register	CAPR	CAPRH	R	Undefined
0C8			CAPRL		Undefined
0C7	Capture input control register		CAPCON	R/W	0FCH
0C6	Serial port buffer		SBUF		Undefined
0C5	Serial port control register	SCON	SCONH		0F0H
0C4			SCONL		00H
0C3	Timer 3 register		T3R		Undefined
0C2	Timer 3 counter		T3C		Undefined
0C1	Timer 3 control register		T3CON		0F4H

ADDRESSING MODES

MSM65512 has 384 bytes of local memory space and 64 Kbytes of general memory space. A variety of addressing modes are available for accessing these spaces.

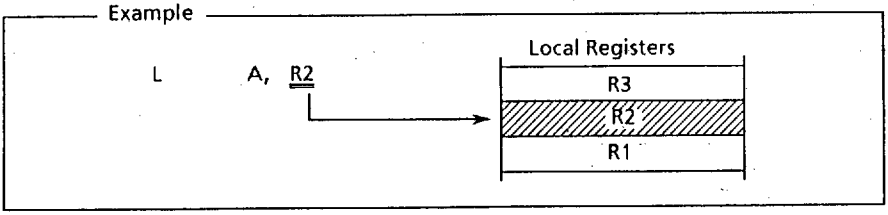
1. Register Direct Addressing

   - A、B、SP、PSW
   - BA



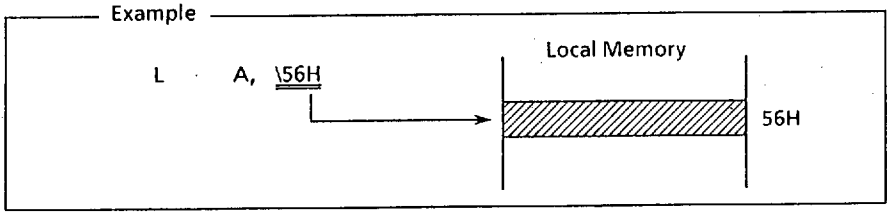
2. Local Register Direct Addressing

   - Rn (n = 0~15)
   - ERn (n = 0, 1)



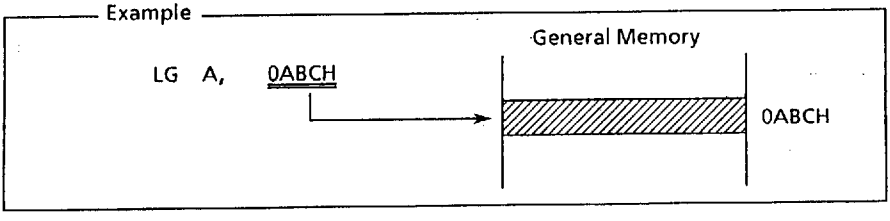
3. Local Memory Direct Addressing

   - \adrs (within 256-byte page; page specified by LMP flag)
   - adrs (384 bytes)



4. General Memory Direct Addressing

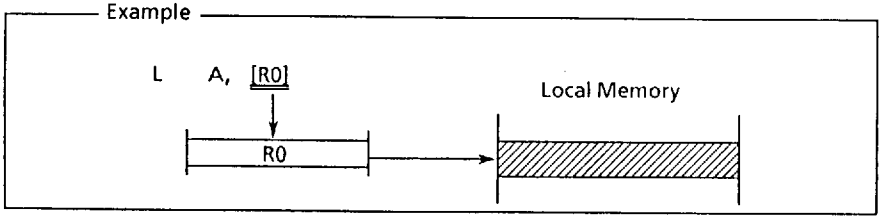
   - adrs



5. Local Memory - Register Indirect Addressing

- [Rn] (n = 0, 1, 8, 9; within 256-byte page; page specified by LMP flag)
- page: [Rn] (page = 0, 1 n = 0, 1, 8, 9 384 bytes)

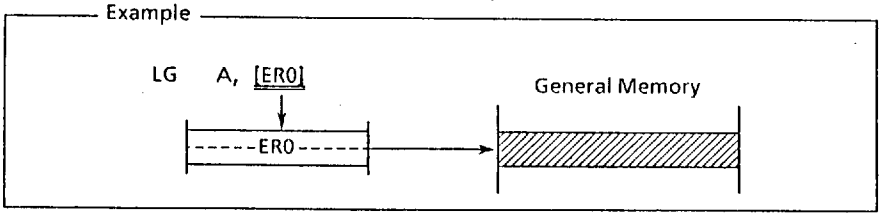
Example



6. General Memory - Register Indirect Addressing

- [ERn] (n = 0, 1)
- [BA]

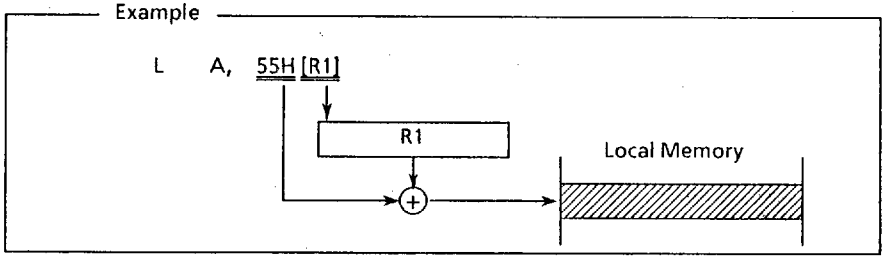
Example



7. Local Memory Index Addressing

- disp [Rn] (n = 1, 9; within 256-byte page; page specified by LMP flag)
- page: disp [Rn] (page = 0, 1 n = 1, 9 384 bytes)

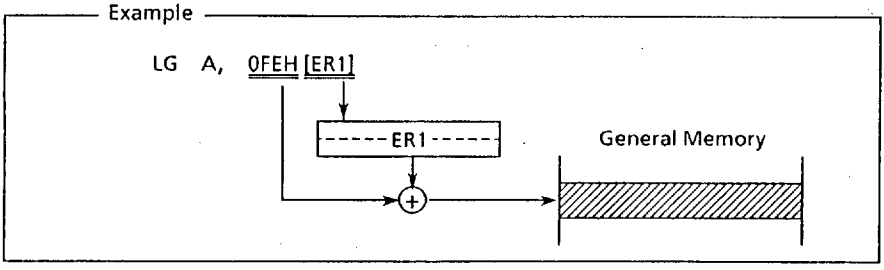
Example



8. General Memory Index Addressing

- disp [ER1]

Example



9. Immediate Addressing

- #n

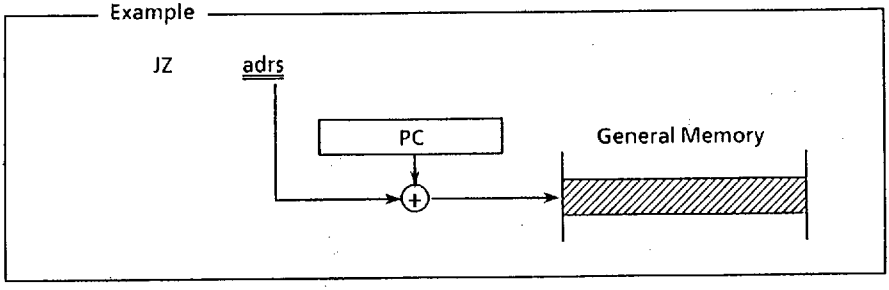
Example

```
L    A, #255
```

10. PC Relative Addressing

- adrs

Example



INSTRUCTION TABLES

• Data Transfer Instructions

Mnemonic		Function
L	obj1, obj2	Local memory load
LG	obj1, obj2	General memory load
ST	obj1, obj2	Store into local memory
STG	obj1, obj2	Store into general memory
MOV	PSW, #n	Immediate data transfer to PSW
MOV	obj1, obj2	Data transfer
MOVG	obj1, obj2	General memory data transfer
MOVW	obj1, obj2	16-bit data transfer
XCH	C, P	Carry and parity exchange
XCH	obj1, obj2	Data exchange
SWAP	obj	Upper nibble and lower nibble swap

• Increment and Decrement

Mnemonic		Function
INC	obj	Data increment
INCG	obj	General memory increment
INCW	obj	16-bit data increment
DEC	obj	Data decrement
DECG	obj	General memory decrement
DECW	obj	16-bit data decrement

• Arithmetic Operations

Mnemonic		Function
ADD	obj1, obj2	Data add
ADDW	obj1, obj2	16-bit data add
ADC	obj1, obj2	Data add with carry
ADCG	obj1, obj2	General memory data add with carry
SUB	obj1, obj2	Data subtract
SUBW	obj1, obj2	16-bit data subtract
SBC	obj1, obj2	Data subtract with carry
SBCG	obj1, obj2	General memory data subtract with carry
MUL		Multiplication 16 ← 8 x 8
DIV		Division 16 ← 16/8, 8 ← 16 mod 8

• Comparisons

Mnemonic		Function
CMP	obj1, obj2	Data compare
CMPW	obj1, obj2	16-bit data compare

• Logical Operations

Mnemonic		Function
AND	PSW, #n	PSW and immediate data logical AND
AND	obj1, obj2	Data logical AND
OR	PSW, #n	PSW and immediate data logical OR
OR	obj1, obj2	Data logical OR
XOR	obj1, obj2	Data exclusive OR

• Bit Operations

Mnemonic		Function
SB	obj. n	Bit set
SB	obj	PSW bit set
RB	obj. n	Bit reset
RB	obj	PSW bit reset
CPL	C	Carry complement
L	C, obj	Bit transfer to carry
ST	C, obj	Bit transfer from carry

• Rotate and Shift

Mnemonic		Function
ROL	obj	Rotate left
ROR	obj	Rotate right
SLL	obj	Shift left
SRL	obj	Shift right

• Decimal Adjust

Mnemonic		Function
DAA	obj	Decimal adjust after add
DAS	obj	Decimal adjust after subtract

• Conditional Jumps

Mnemonic		Function
JZ	adrs	Jump if zero flag is set
JNZ	adrs	Jump if zero flag is not set
JC	adrs	Jump if carry is set
JNC	adrs	Jump if carry is not set
DJZ	Rn, adrs	Decrement register, and jump if zero
DJNZ	Rn, adrs	Decrement register, and jump if not zero
JBS	obj. n, adrs	Jump if bit is set
JBR	obj. n, adrs	Jump, if bit is reset
JBSC	obj. n, adrs	Jump and clear bit if bit is set
CJE	C, P, adrs	Compare carry and parity; jump if equal
CJNE	C, P, adrs	Compare carry and parity; jump if not equal
CJE	obj1, obj2, adrs	Compare; jump if equal
CJNE	obj1, obj2, adrs	Compare; jump if not equal
CJEG	obj1, obj2, adrs	Compare with general memory data; jump if equal
CJNEG	obj1, obj2, adrs	Compare with general memory data; jump if not equal

• Jumps

Mnemonic		Function
J	adrs	Jump
SJ	adrs	Short jump
J	[BA]	Indirect jump

• Subroutines

Mnemonic		Function
PUSH	obj	Data push
POP	obj	Data pop
CAL	adrs	Subroutine call
CALZ	adrs	Call subroutine if zero flag is set
CALC	adrs	Call subroutine if carry flag is set
VCAL	n	Vector call
VCALZ	n	Vector call if zero flag is set
VCALC	n	Vector call if carry flag is set
RT		Return from subroutine
RTZ		Return from subroutine if zero flag is set
RTC		Return from subroutine if carry flag is set

• Other Instructions

Mnemonic		Function
CLR	obj	Clear
CLRW	BA	16-bit data clear
CPL	obj	Data complement
CPLW	BA	16-bit data complement
NOP		No operation
CHK	obj	Parity check
DLY	n	Program execution delay

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Ta = 25°C	− 0.3~7.0	V
Input voltage	V_I		− 0.3~V_{DD} + 0.3	
Output voltage	V_O		− 0.3~V_{DD} + 0.3	
Power dissipation	P_D	Ta = 25°C (per package)	400	mW
		Ta = 25°C (per output)	50	
Storage temperature	T_{STG}	—	− 55~ + 150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	$f_{OSC} \leqq$ 10MHz	4.5 ~ 5.5	V
Memory hold voltage	V_{DDMH}	f_{OSC} = 0 Hz	2 ~ 5.5	
Operating frequency	f_{OSC}	V_{DD} = 5V ± 10%	0 ~ 10	MHz
Operating temperature	T_{OP}	—	− 40 ~ + 85	°C

DC CHARACTERISTICS

(V_{DD} = 5V ± 10%, GND = 0 V, Ta = − 40~ + 85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
"H" input voltage 1 *1	V_{IH1}	—	2.4	–	V_{DD} + 0.3	V
"H" input voltage 2 *2	V_{IH2}	—	0.7 V_{DD}	–	V_{DD} + 0.3	
"L" input voltage	V_{IL}	—	− 0.3	–	0.8	
"H" output voltage 1 *3	V_{OH1}	I_{OH} = − 200μA	0.75V_{DD}	–	–	
"H" output voltage 2 *4	V_{OH2}	I_{OH} = − 400μA	0.75V_{DD}	–	–	
"L" output voltage 1 *3	V_{OL1}	I_{OL} = 1.6mA	–	–	0.4	
"L" output voltage 2 *4	V_{OL2}	I_{OL} = 3.2mA	–	–	0.4	
Input leak current 1 *5	I_{LI1}	V_I = V_{DD}/0V	–	–	± 1	μA
Input leak current 2 *6	I_{LI2}	V_I = V_{DD}/0V	–	–	± 10	
"L" input current *7	I_{IL}	V_I = 0V	− 40	− 200	− 400	
Input capacity	C_I	f = 1 MHz, Ta = 25°C	–	5	–	pF
Current consumption	I_{DDS}	Stop mode **	–	–	50	μA
Current consumption (MSM65512)	I_{DD}	$f_{(OSC)}$ = 10MHz, no load	–	15	30	mA
Current consumption (MSM65P512)	I_{DD}	$f_{(OSC)}$ = 10MHz, no load	–	20	40	

* 1: Excluding OSC0 and $\overline{RESET}$

* 2: OSC0 and $\overline{RESET}$

* 3: Excluding P0, ALE, $\overline{RD}$, P2.6/$\overline{WR}$

* 4: P0, ALE, $\overline{RD}$, P2.6/$\overline{WR}$

* 5: $\overline{EA}$

* 6: Excluding $\overline{RESET}$, $\overline{EA}$

*7: $\overline{RESET}$

** : The ports set for input mode are V_{DD} or 0V and the ports except these are no load.

AC CHARACTERISTICS

• External Memory Control

($V_{DD} = AV_{DD} = 5V \pm 10\%$, $GND = AGND = 0V$ $Ta = -40 \sim +85°C$)

Parameter	Symbol	Condition	Min	Max	Unit
Clock period	t_C	—	100	–	nS
"L" clock pulse width	t_{CLW}		45	–	
"H" clock pulse width	t_{CHW}		45	–	
ALE pulse width	t_{AW}	$C_L = 100pF$	$t_C + t_{CHW} - 20$	–	
ALE pulse delay time 1	t_{ALD1}		$t_{CLW} - 20$	–	
ALE pulse delay time 2	t_{ALD2}		$t_{CLW} - 20$	–	
$\overline{RD}$ pulse width	t_{RW}		$t_C + t_{CHW} - 20$	–	
$\overline{RD}$ pulse delay time	t_{RD}		$t_{CLW} - 20$	$t_{CLW} + 20$	
$\overline{WR}$ pulse width	t_{WW}		$t_C + t_{CHW} - 40$	–	
$\overline{WR}$ pulse delay time	t_{WD}		$t_{CLW} - 20$	$t_{CLW} + 40$	
"L" address set up time	t_{LAS}		$t_C - 40$	–	
"H" address set up time	t_{HAS}		$t_C - 40$	–	
"L" address hold time	t_{LAH}		$t_{CLW} - 20$	–	
Bus float time	t_{LAZ}		–	20	
"H" address hold time	t_{HAHR}		$t_C - 20$	–	
"H" address hold time	t_{HAHW}		$t_C - 20$	–	
Read data access time	t_{RDAA}		–	$t_C + t_{CLW} - 15$	
Read data access time	t_{RDAR}		–	$t_{CHW} + 10$	
Read data hold time	t_{RDH}		0	–	
Write data set up time	t_{WDS}		$t_C + t_{CHW} - 40$	–	
Write data hold time	t_{WDH}		$t_{CLW} - 20$	–	

• CPU Control

(V_{DD} = 5V ± 10%, GND = 0V, Ta = −40~ +85°C)

Parameter		Symbol	Condition	Min	Max	Unit
$\overline{\text{RESET}}$ pulse width 1	*1	t_{RESW1}	—	20	—	nS
$\overline{\text{RESET}}$ pulse width 2	*2	t_{RESW2}	—	*3	—	—

*1 Excluding power ON, stop mode and hard stop mode

*2 In power ON, stop mode and hard stop mode

*3 Oscillation stabilization time depends on resonator

• Peripheral Control 1

(V_{DD} = 5V ± 10%, GND = 0V, Ta = −40~ +85°C)

Parameter		Symbol	Condition	Min	Max	Unit
OSC	Clock period	t_C	—	100	—	nS
EXI	External interrupt pulse width	t_{EXIW}	—	4 t_C	—	
T0	External clock pulse width	t_{T0CW}		4 t_C	—	
	GATE pulse width	t_{T0GW}		1 t_{T0CLK} *	—	
T2	External clock pulse width	t_{T2CW}		4 t_C	—	
CAP	CAP pulse width	t_{CAPW}		12 t_C	—	

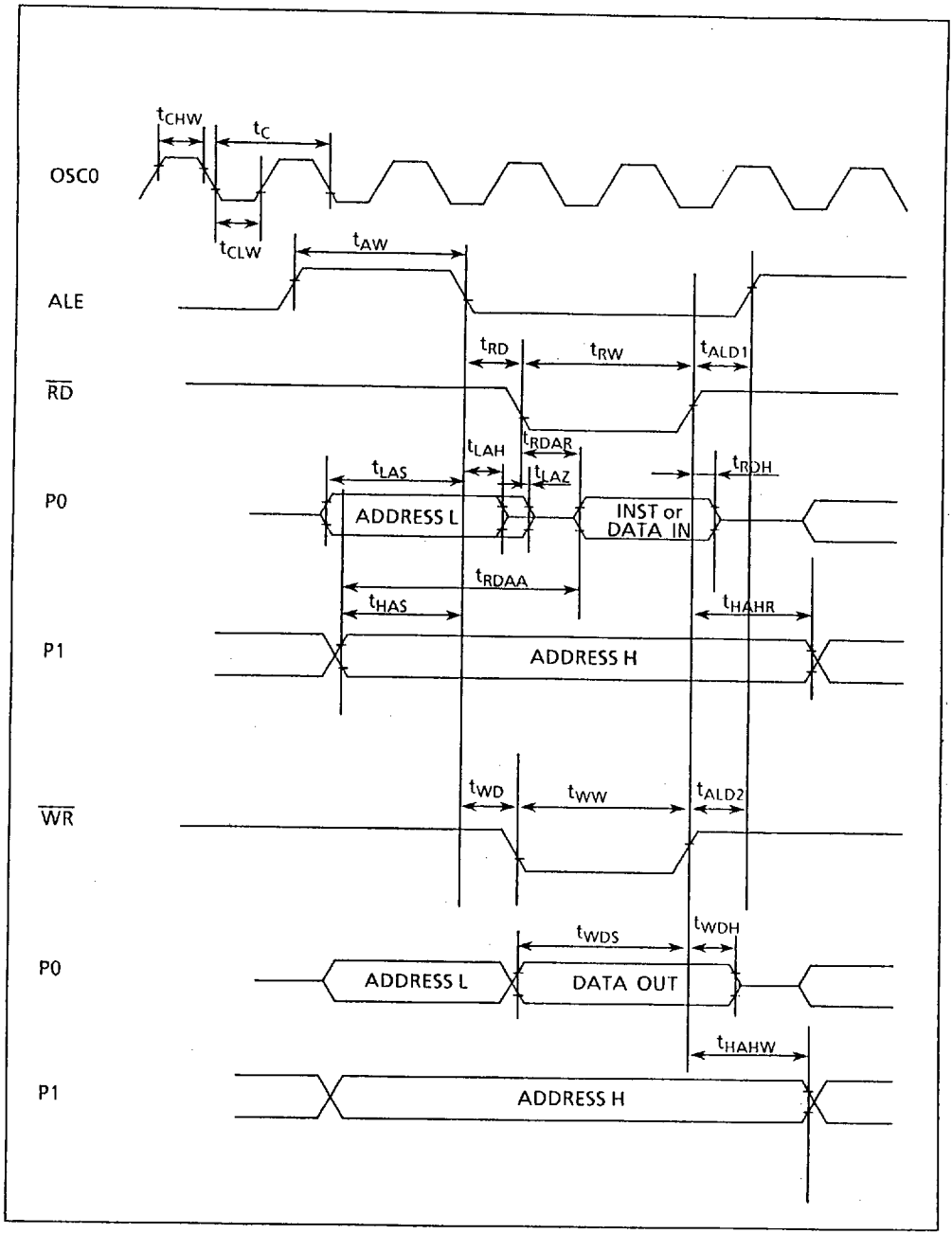
* t_{T0CLK}: Timer 0 count clock period selected by T0CON

• Peripheral Control 2

(V_{DD} = 5V ± 10%, GND = 0V, Ta = −40~ +85°C)

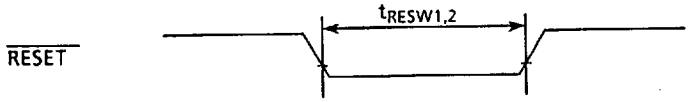
Parameter		Symbol	Condition	Min	Max	Unit
OSC	Clock period	t_C	—	100	—	nS
SFT	SFTCK period	t_{SFC}	C_L = 100pF	8 t_C	—	
	SFTCK "L" pulse width	t_{SFCLW}		4 t_C − 20	—	
	SFTCK "H" pulse width	t_{SFCHW}		4 t_C − 20	—	
	SFTO set up time	t_{SFOS}		t_{SFCLW} − 100	—	
	SFTO hold time	t_{SFOH}		t_{SFCHW} − 100	—	
	SFTI set up time	t_{SFIS}		100	—	
	SFTI hold time	t_{SFIH}		100	—	
SIO (Clock synch-ronous mode)	Synchronous clock period	t_{SIC}		8 t_C	—	
	Synchronous clock "L" pulse width	t_{SICLW}		4t_C − 20	—	
	Synchronous clock "H" pulse width	t_{SICHW}		4t_C − 20	—	
	Output data set up time	t_{SIOS}		6t_C − 100	—	
	Output data hold time	t_{SIOH}		2t_C − 100	—	
	Input data set up time	t_{SIIS}		t_C + t_{CLW} + 100	—	
	Input data hold time	t_{SIIH}		0	—	

- **External Memory Control**

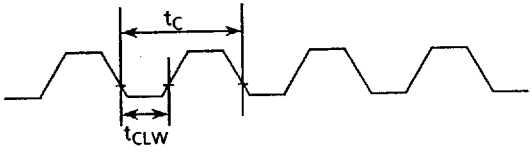


• CPU Control

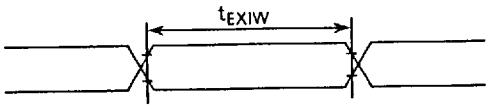
1) $\overline{\text{RESET}}$ Pulse width



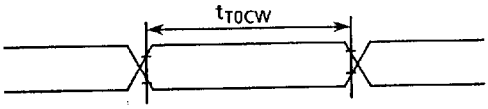
• Peripheral Control 1

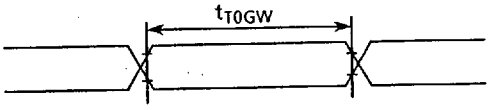


1) EXI Pulse width

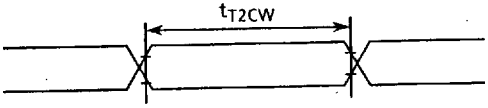


2) T0

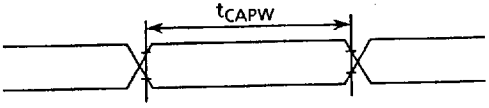




3) T2

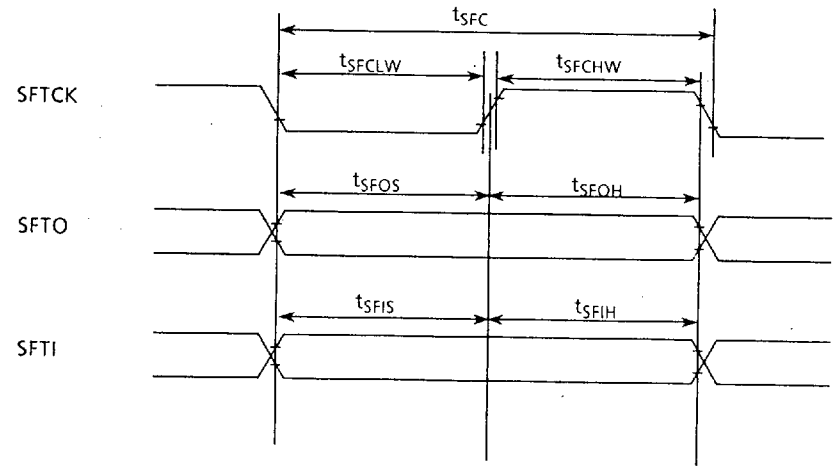


4) CAP



• Peripheral Control 2

1) SFT



2) SIO
(Clock synchronous mode)