MOTHERBOARD CLOCK GENERATOR

FEATURES

- Clock generator for IBM[TM] PC/AT system
- Mask programmable CPU clock up to 80 MHz
- Provides three clock outputs (14.318 MHz, 24MHz, and a CPU clock)
- Built-in advanced PLL for low phase-jitter, driven by a 14.318 MHz crystal

- Provides low power mode
- Under 0.1% CPU clock period change while switching frequencies.
- Package
  - 14-pin PDIP
  - 14-pin SOP

GENERAL DESCRIPTION

The MX8315 is a CMOS motherboard clock generator used in PC system to eliminate the need for additional crystal oscillators to reduce the overall system cost.

The MX8315 is capable of generating three clock outputs , a 14.318MHz master clock output , a 24 MHz peripherial clock, and a programmable CPU clock. If a different set of frequencies (range from 10 MHz to 80 MHz), or peripherial clock (8, 16, or 24 MHz) is re-

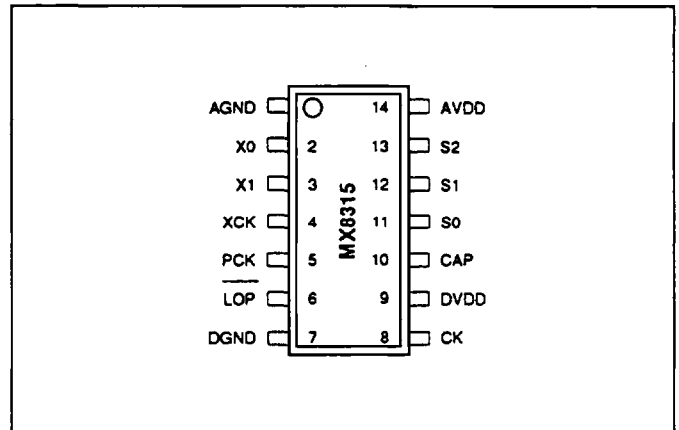quired, MXIC can make a custom version by changing one mask layer.

The clock chip features smooth and glitch-free frequency transitions when select pins are changed or low power mode is enable. The chip meets the 486 specifications of subsequent clock period changed under 0.1%.
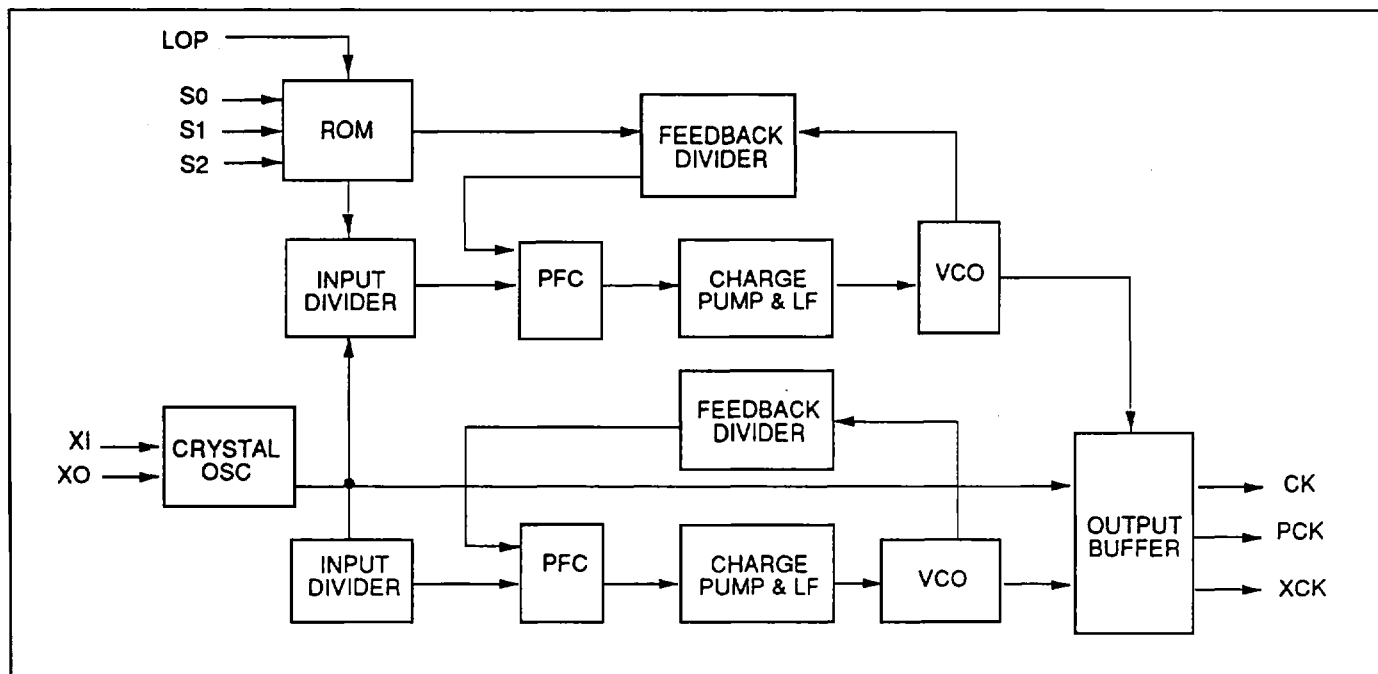
PIN CONFIGURATIONS

14 PDIP
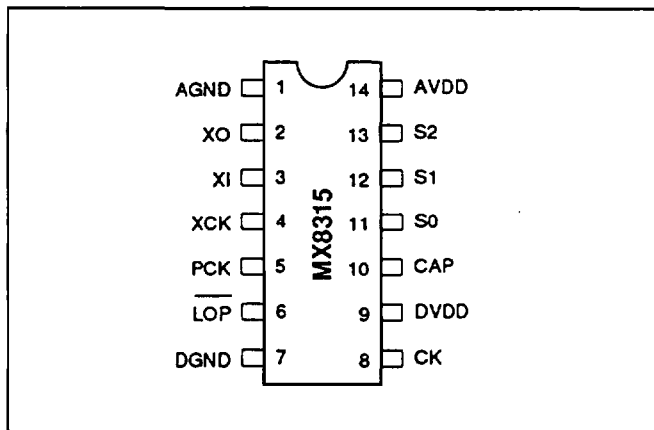
14 SOP

BLOCK DIAGRAM

PIN DESCRIPTION

| SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
AGND		1	Analog ground
XO	O	2	Xtal Output. No connection during clock input
XI	I	3	Xtal input or reference clock input
XCK	O	4	Xtal clock output (14.318MHz)
PCK	O	5	Peripheral clock output (24MHz)
LOP	I	6	Internal pull high input. When asserted low, the output frequency of CK gradually transits to 8 MHz
DGND		7	Digital ground
CK	O	8	CPU clock output
DVDD		9	Digital power supply
CAP		10	Loop filter capacitor
S0	I	11	Frequency select 0. Internal pull high
S1	I	12	Frequency select 1. Internal pull high
S2	I	13	Frequency select 2. Internal pull high
AVDD		14	Analog power supply

FUNCTIONAL DESCRIPTION

The MX8315 mother-board clock generator is an integrated circuits of phase-lock loop frequency synthesizer capable of generating three clock signals for the PC system. XCK (pin 4) provides the crystal oscillation frequency (14.31818MHz). PCK (pin5) provides the peripheral device frequency (24MHz). CK(pin8) provides CPU frequency, which can be programmable through three select pins (S0, S1 and S2) based on the frequency table shown below.

The MX8315 minimizes the pin number and external component number. As shown in the block diagram, the major functional blocks are the ROM, feedback and input dividers, phases frequency comparator (PFC), charge pump circuitry, voltage-controlled oscillator (VCO) and crystal oscillator.

LOOP FILTER

The MX8315 minimizes the external number of resistor and capacitor which are required for conventional loop filter. In this chip only a capacitor is required.
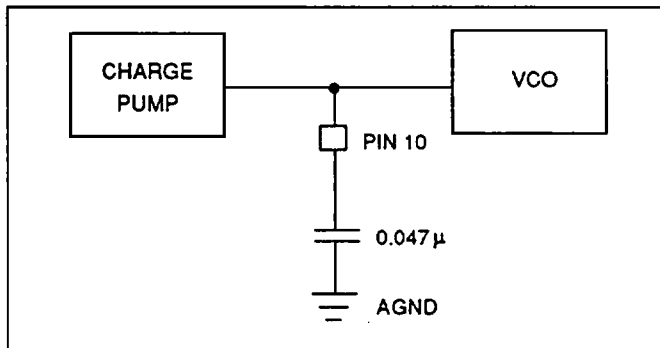
FREQUENCY TABLE

S2	S1	S0	CK(MHz)
0	0	0	33.33
0	0	1	80
0	1	0	66.67
0	1	1	50
1	0	0	40
1	0	1	60
1	1	0	25
1	1	1	20

FREQUENCY REFERENCE

The internal reference oscillator includes all passive components required. A proper resonant crystal should be connected between the X0 (pin 2) and X1 (pin 3). Crystal range from 10 MHz to 25 MHz is recommended. A 14.31818 MHz crystal, however, is usually used. To minimize the noise pickup, maintain short lead lengths between the crystal and MX8315 by soldering the crystal to the ground plane. The reference clock can also be supplied by external clock signal. In this case, the XI should be connected to reference clock and XO be disconnected. The decoupling capacitors and the loop filter capacitor connected to MX8315 should be as close as possible to reduce noise susceptibility.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Storage Temperature	-85°C to 150°C
Applied Input Voltage	-0.5V to VDD + 0.5V
Applied Output Voltage	-0.5V to VDD + 0.5V
Supply Voltage	-0.5V to 7V
Operating Temperature	0 to 70°C
Power Dissipation	0.5 Watts

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXI-MUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
NOTICE:
Specifications contained within the following tables are subject to change.

## DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VDD, AVDD	Supply Voltage	4.5	5	5.5	V	
IDD	Supply Current		TBD		mA	No load, running at 80 MHz
VOL	Output Low Voltage			0.4	V	CK1 and CK2 IOL=20mA
VOL	Output Low Voltage			0.4	V	XCK, IOL=5mA
VOH	Output High Voltage	2.4			V	CK1 and CK2 IOH=-45mA
VOH	Output High Voltage	2.4			V	XCK, IOH=-15mA
RPU	Pull up Resistor			80K	Ohms	

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		8		pF	
COUT	Output Capacitance		8		pF	

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Tr	Rise Time (0.8V-2.0V)			2	ns	25 pF load
Tf	Fall Time (2.0V-0.8V)			2	ns	25 pF load
Dt	Output Duty Cycle	45/55	50/50	55/45		25 pF load
Fref	Reference Clock Frequency		14.31818		MHz	
Tref	Reference Clock Period		69.8412		ns	

WAVEFORMS
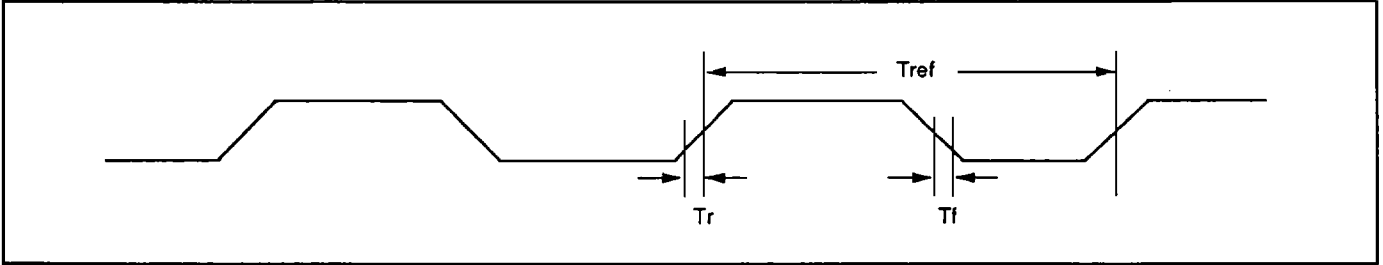
ORDERING INFORMATION
PLASTIC PACKAGE

PART NO.	PACKAGE
MX8315PC	14-PIN DIP
MX8315MC	14-PIN SOP

PACKAGE INFORMATION

14-PIN PLASTIC DIP (300 mil)

ITEM	MILLIMETERS	INCHES
A	19.43 max.	.765 max.
B	1.90 [REF]	.075 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	15.24	.600
F	1.52 [Typ.]	.060 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.30 ± .25	.130 ± .010
J	4.32 ± .25	.170 ± .010
K	7.61 ± .25	.300 ± .010
L	6.48 ± .25	.255 ± .010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.
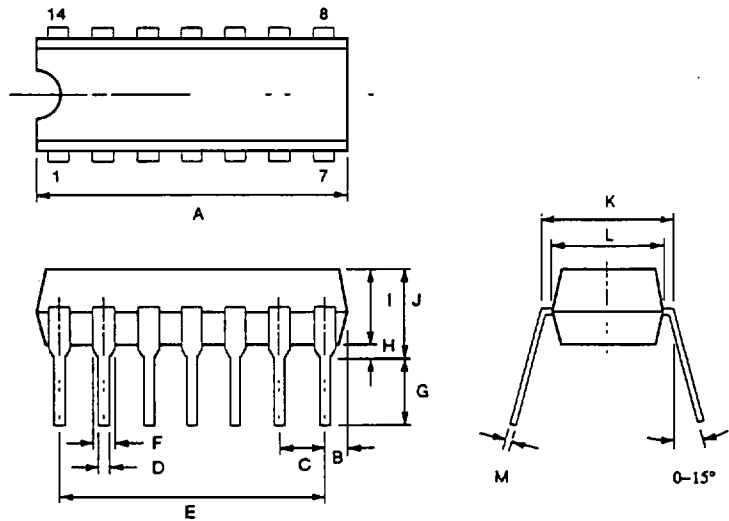
14-PIN PLASTIC SOP (150 mil)

ITEM	MILLIMETERS	INCHES
A	8.89 max.	.350 max.
B	.76	.030 [REF]
C	1.27 [TP]	.050 [TP]
D	.41 [Typ.]	.016 [Typ.]
E	.10 min.	.004 min.
F	1.91 max.	.075 max.
G	1.42 ± .13	.056 ± .005
H	5.99 ± .3	.236 ± .012
I	3.91 ± .13	.154 ± .005
J	1.02	.040
K	.20 [Typ.]	.008 [Typ.]
L	.76	.030

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.
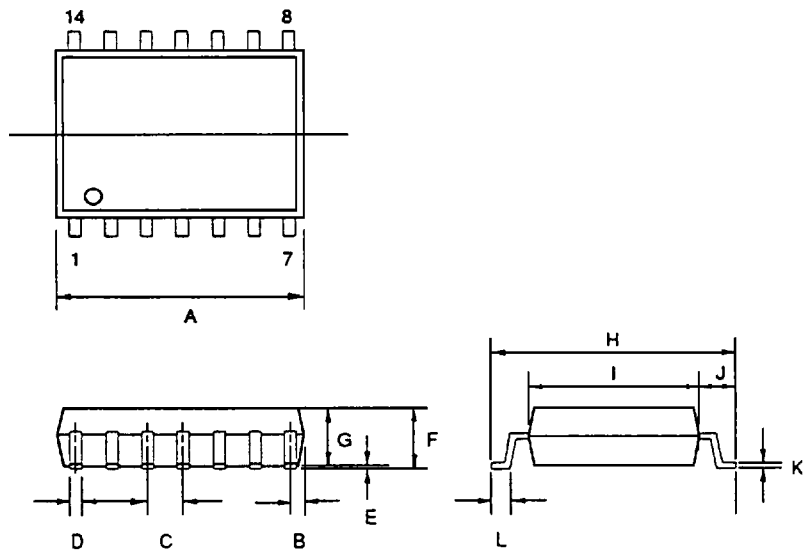
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