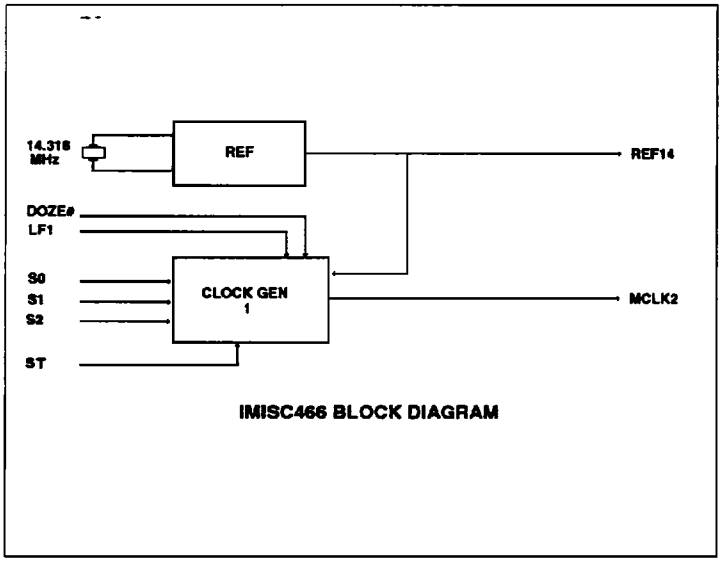
IMISC466 SYSTEM CLOCK CHIP

March 1994
Preliminary

CMOS LSI
PLL FREQUENCY SYNTHESIZER

PRODUCT FEATURES

- Generates All Essential Clock Signals for the Motherboards
- 4V to 7V Operating Supply Range
- Supports 8086, 80286, 80386 and 80486 including S Series ® and Pentium ® Based Designs
- Supports ISA, VESA, and PCI Based Designs
- Supports GREEN PC applications
- Integrates Clock, CPU Clock and Buffered 14.318 MHz Output
- Wide Range of Selectable Output Frequencies Including 80, 66.6, 60, 50, 40, 33.3, 30, 25, 16 and 8 MHz
- Doze Mode for Low Power Consumption
- Single, Low Cost Crystal (14.318 MHz) Used as Reference Frequency
- Smooth and Glitch-Free Switching for Programmable Clock Generator
- 50% Duty Cycle
- TTL or CMOS Compatible Outputs
- Low, Short and Long Term Jitter
- 14 PDIP



IMISC466 BLOCK DIAGRAM

PRODUCT DESCRIPTION

The IMISC466 is a clock chip for Motherboards. The IMISC466 uses a single 14.318 MHz external crystal to generate all essential clock signals. The IMISC466 is designed to generate CPU clock options of 80 MHz, 66.6 MHz, 60 MHz, 50 MHz, 40 MHz, 33.3 MHz, 30 MHz, 20 MHz, 16 MHz and 8 MHz, giving flexibility to the user. The frequency selection on the MCLK outputs is determined by the S0-S2 pins. DOZE# pin give additional flexibility to the user for Green PC applications. Activating the DOZE# pin smoothly switches the MCLK output to preprogrammed DOZE frequencies. Deactivating the DOZE input allows the CPU output to return to full speed.

APPLICATIONS

IMISC466 eliminates the need for multiple oscillators and generates all the essential clock signals for the Personal Computer Motherboards. Supports 8086, 80286, 80386SX, 80386DX, 80486SX, 80486DX, 80486DX2, 80486 S Series ®, and Pentium ® based designs. IMISC466 can be used with Green PC, laptop or notebook computers to save power by running the system slower than normal CPU speeds.

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MILPITAS, CA 95035 TEL :408-263-6300 FAX : 408-263-6571

IMCIS049

PIN DESCRIPTION

OSCin, OSCout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCin may also serve as input for an externally generated reference signal.

S0, S1, and S2 - Standard frequency select inputs. These inputs control the high speed MCLK frequency selection. S0-S2 inputs control the CPU clock frequencies. All these inputs have internal pull-ups.

Table 1 shows the output frequency selection conditions.

MCLK - Master clock output. Programmable output frequencies can be selected using S0-S2 inputs shown in Table 1.

DOZE# - DOZE control pin. When DOZE# is high, the clock chip operates in the standard mode. When this pin goes low, output frequencies are switched to the pre-programmed DOZE frequencies. Switching to DOZE frequencies occur smoothly to allow tracking by 486 CPU internal PLL. This pin has an internal pull-up.

REF14 - 14.31818 MHz output. Buffered output of on-chip reference oscillator or externally provided reference.

ST - Doze frequency select input. This pin set the Doze frequency for MCLK outputs when DOZE# goes low. This input has internal pull-ups. Four Doze frequencies can be programmed.

LF1 - This is the phase detector output for the clock generator. It is single-ended, tri-state output for use as loop error signal. A 0.1uF capacitor to ground should be connected from this pin to form the loop filter.

VSS - Circuit ground.

VDD - Positive power supply.

AVSS - Analog circuit ground.

AVDD - Analog positive power supply.

SC466 FREQUENCY TABLE

INPUTS			MCLK OUTPUT (MHz)		
S2	S1	S0	DOZE# = 1	DOZE# = 0	
				ST = 1	ST = 0
0	0	0	66.6	33.3	16
0	0	1	80	16	8
0	1	0	60	33.3	16
0	1	1	30	8	4
1	0	0	33.3	8	4
1	0	1	40	8	4
1	1	0	50	8	16
1	1	1	25	8	8

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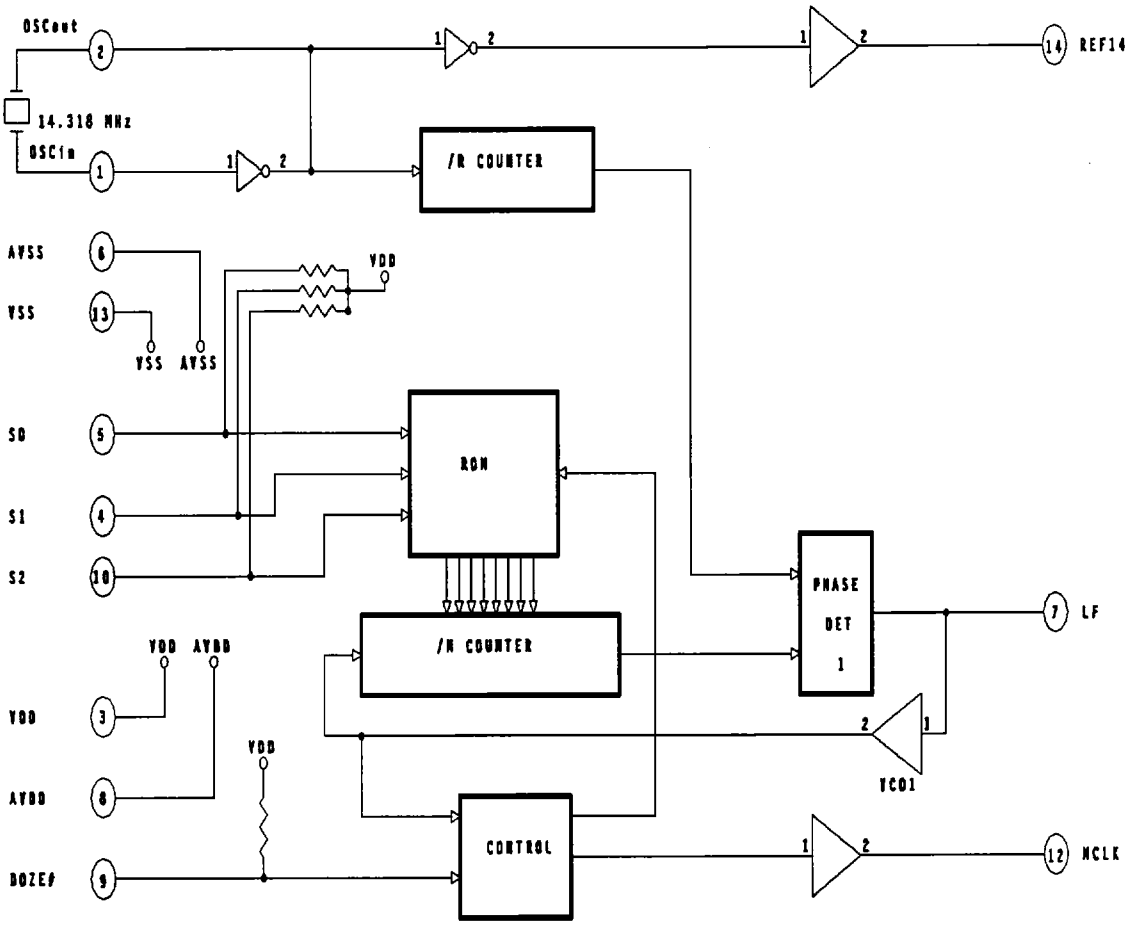
BLOCK DIAGRAM



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IMI SC466 BLOCK DIAGRAM

MAXIMUM RATINGS

Voltage Relative to VSS : -0.3V to 7V

Voltage Relative to VDD : 0.3V

Storage Temperature : -65°C to +150°C

Ambient Temperature: -55°C to +125°C

Recommended Operating Range: 4V - 7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	V_{IL}	-	-	0.8	Vdc	S0-S2 Inputs
Input High Voltage	V_{IH}	2.0	-	-	Vdc	S0-S2 Inputs
Input Low Current With Pull-up or Pull-down	I_{IL}	-	-	5 ±50	uA	S0-S2 Inputs
Input High Current With Pull-up or Pull-down	I_{IH}	-	-	5 ±50	uA	S0-S2 Inputs
Output Low Voltage I_{OL} = 12mA	VOL	-	-	0.4	Vdc	All Other Outputs
Output High Voltage I_{OH}= 12mA	VOH	2.4	-	-	Vdc	All Other Outputs
Tri-State Leakage Current	Ioz	-	-	10	uA	LF1, LF2 and LF3
Dynamic Supply Current	Icc	-	-	35	mA	VDD @ 5V, MCLK2 = 50 MHz
Short Circuit Current	Isc	25	-	-	mA	
						VDD = 5V ±10%, TA = 0°C to +70°C

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SWITCHING CHARACTERISTICS

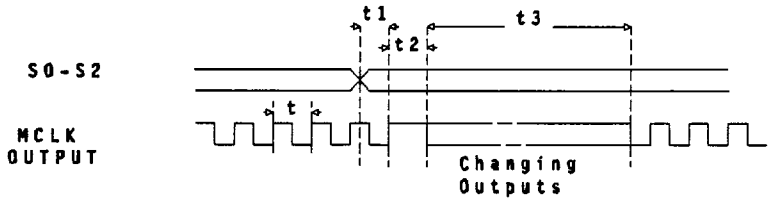
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) Time All Outputs	t_{TLH}, t_{THL}	-	-	2	ns	30 pf Load
Duty Cycle MCLK and REF14		-	50/50	45/55	%	
Jitter One Sigma MCLK and REF14	t_{j1s}	-	-	± 2	%	As Compared with Clock Period
Jitter Absolute MCLK and REF14	t_{jab}	-	-	± 5	%	As Compared with Clock Period
Input Rise/Fall Time S0-S3		-	-	2	us	
						VDD = 5V ±10%, TA = 0°C to 70°C

OSCILLATOR CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Transconductance	gm	20	330		millimhos	@ 14.3 MHz
Output Impedance	Z_o	-	200	800	ohms	@ 14.3 MHz
Input Capacitance	Ci	8	13	18	pf	
Output Capacitance	Co	3	6	9	pf	
DC Bias Voltage	V_B	1.5	VDD/2	3.5	Volt	
Start-up Time	ts	-	-	10	ms	@ 14.3 MHz
Input Rise Time OSCIN	ICLKr	-	-	2	us	
Input Fall Time OSCIN	ICLKf	-	-	2	us	
						VDD = 5V ±10%, TA = 0°C to 70°C

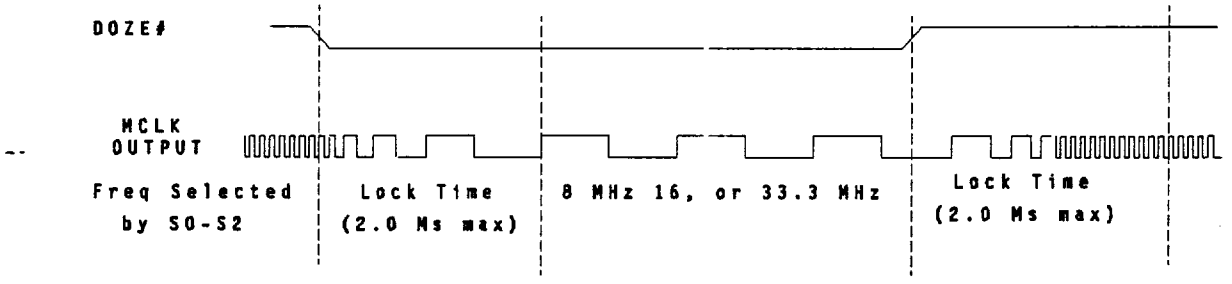
TIMING DIAGRAMS

STANDARD MODE



t : Current cycle time
t1: time to first positive edge after address change
t2: Output high time. t2 = 4t
t3: Lock time. 2.0ms max

DOZE MODE
(MCLK2: Switching to 8 MHz 16 MHz or 33.3 MHz)



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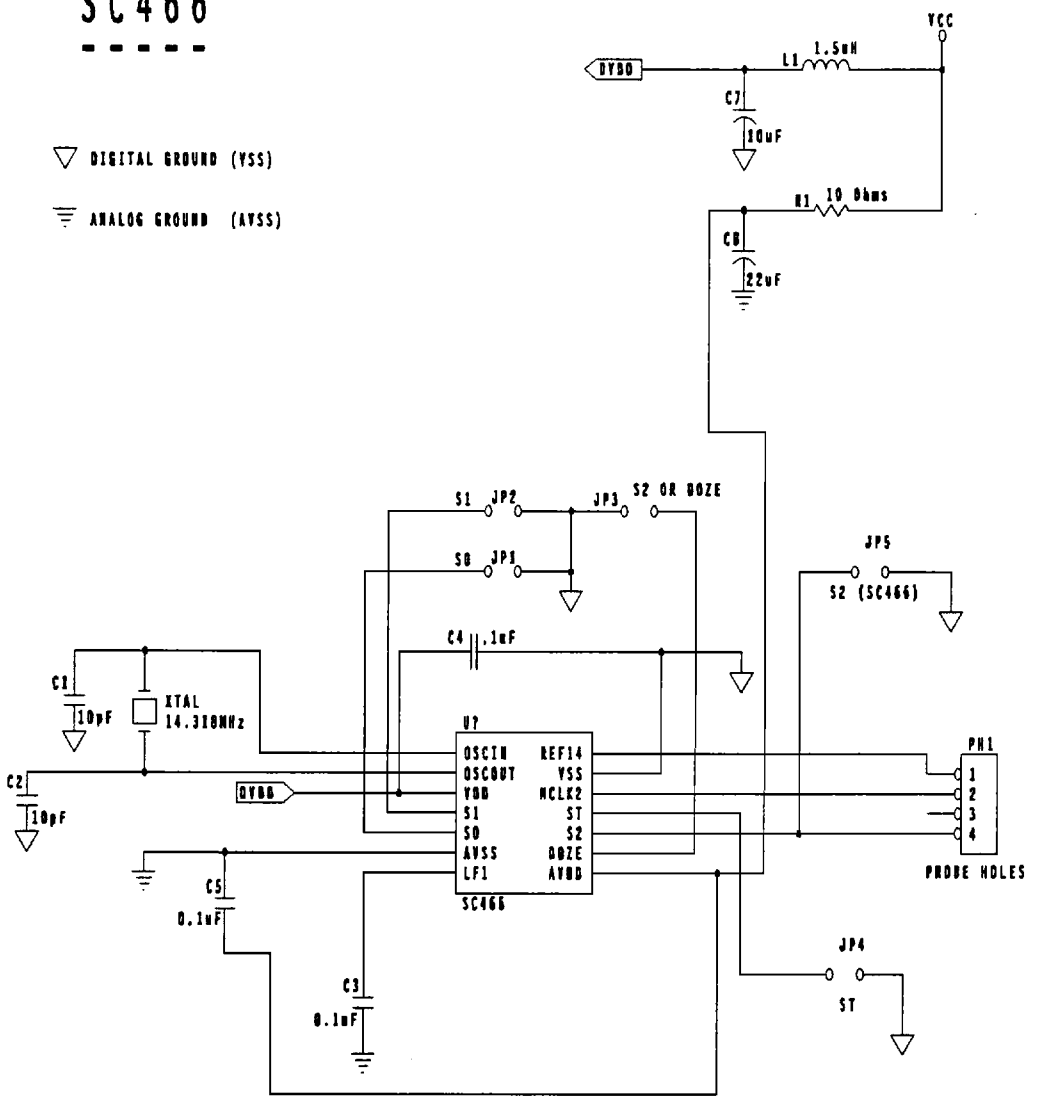
APPLICATION SUGGESTION



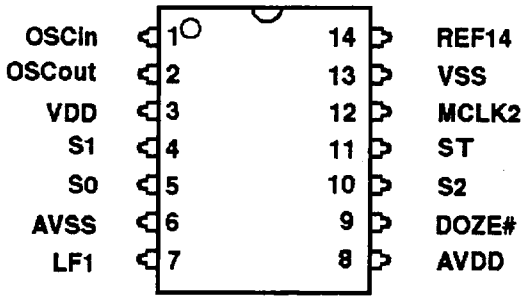
NOTE1: C0,C3,C4,C6,C7 MUST BE CLOSE TO THEIR PINS

NOTE2: R0 MUST BE CLOSE TO ITS PIN

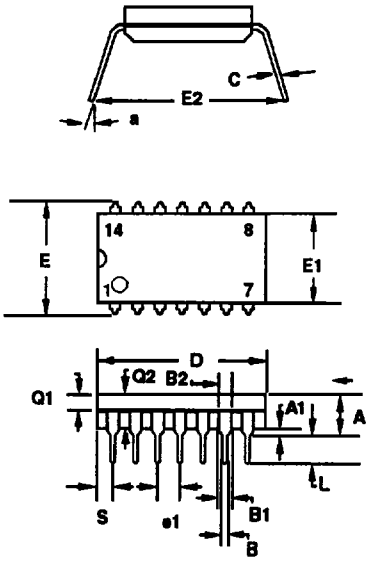
NOTE3: CONNECT DIGITAL GROUND AND ANALOG GROUND THROUGH ONE POINT ONLY ON PC BOARD

NOTE4: C5,C8, AND R1 MUST BE CLOSE TO AVDD AND AVSS

CONNECTION DIAGRAM FOR PLASTIC DIP PACKAGE



PACKAGE DRAWING AND DIMENSIONS



14 PLASTIC DIP

14 PIN SKINNY PLASTIC DIP DIMENSIONS						
SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.145	-	0.155	3.68	-	3.93
A1	0.020	-	-	0.050	-	-
B	0.016	0.018	0.020	.040	.045	.050
B1	0.058	0.060	0.062	1.47	1.52	1.57
B2	0.046	0.049	0.052	1.17	1.24	1.32
C	0.008	0.010	0.012	0.20	0.25	0.30
D	0.748	0.750	0.752	19.0	19.05	19.10
E	0.298	-	0.302	7.57	-	7.67
E1	0.248	0.250	0.252	6.30	6.35	6.40
E2	0.335	0.345	0.355	8.51	8.76	9.01
e1	0.100 BSC			2.54 BSC		
L	0.128	0.130	0.132	3.25	3.30	3.35
a	0°	7°	15°	0°	7°	15°
Q1	0.059	0.060	0.061	1.50	1.53	1.55
Q2	0.128	0.130	0.132	3.25	3.30	3.35
S	0.073	0.075	0.077	1.85	1.90	1.95

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ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC466xPB	Plastic Dip	Commercial, 0°C to +70°C

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC466xPB
Date Code, Lot #

IMISC466xPB

Flow
B = Commercial, 0°C to +70°C

Package
P = Plastic Dip

Revision

IMI Device Number