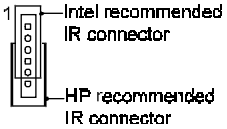
Jumper Setting Quick Reference

J1/J2: Infra Red connector



J4: Hard disk LED header

J5: System reset switch header

J7: Speaker header

J8: Power good LED header

JP1: Green LED header

JP3: ATX Soft power switch header

JP4: Green switch header

JPX2: CMOS data clear setting jumper
2~3 short: Normal (default)
1~2 short: Clear CMOS data

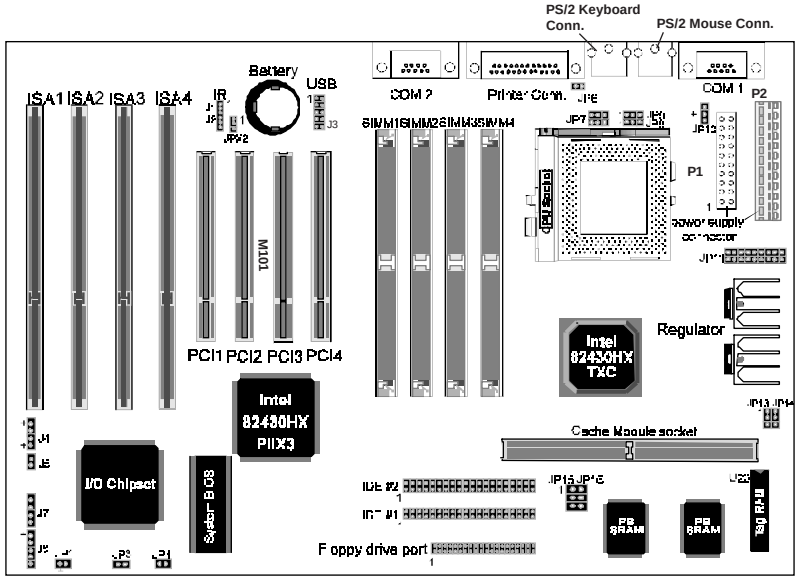
JP6: Keyboard grounding setting jumper
To decrease the EMI radiation, we suggest you open this header after finishing the system assembly.

JP10: CPU cooling Fan header

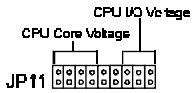
JP15/JP16: External cache size jumper setting

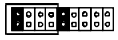
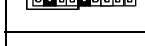
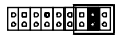
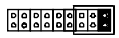
Cache size	Cache on Board	Cache Module	JP15, JP16
256KB	32K*32 x 2	--	
512KB	32K*32 x 2	32K*32 x 2	

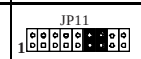
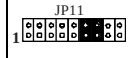
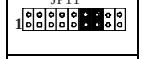
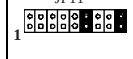
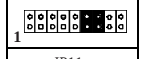
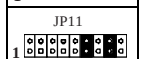
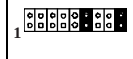
U20: Adding an extra Tag-RAM(32K*8) to expand DRAM cacheable range up to 512MB



For VRT (Voltage Reduction Technology) processor (such as Intel P55C), the split power plan (CPU's core voltage ≠ CPU's I/O voltage) design is required.



CPU Core Voltage			CPU I/O Voltage	
JP7	JP11	Core Vcc	JP11	I/O Vcc
		2.5		3.3
		2.7		
		2.8		3.4
		2.9		3.5

CPU-type		S-spce	CPU Power Voltage			System Frequency		Frequency ratio	
			Vcc	JP7	JP11	MHz	JP13, JP14	Speed rate	JP8, JP9
Intel	P54C-75		3.3	JP7		50		x1.5	
	P54C-90	QO653 QO655 SZ978 SX957 SX959	3.3			60		x1.5	
		QO654 SX958	3.4						
			3.5						
	P54C-120	QO708	3.3					x2	
	P54C-150		3.5					x2.5	
	P54C-100	QO656	3.3			66		x1.5	
		QO657	3.4						
	P54C-133		3.5					x2	
	P54C-166							x2.5	
	P54C-200							x3	
AMD	K5-PR75	ABQ	3.5			50		1.5	
	K5-PR90					60			
	K5-PR100					66			

CPU freq.= Freq. rate x System freq.	JP8	JP9
75/90/100 = 1.5 x system clock	2~3	2~3
110/120/133 = 2 x system clock	2~3	1~2
150/166 = 2.5 x system clock	1~2	1~2
180/200 = 3 x system clock	1~2	2~3

V.2