# CS8221 NEW ENHANCED AT (NEAT™) DATA BOOK
# 82C211/82C212/82C215/82C206 (IPC) CHIPSet™

- **100% IBM™ PC/AT Compatible New Enhanced CHIPSet™ for 12MHz to 16MHz systems**
- **Supports 16MHz 80286 operation with only 0.5-0.7 wait states for 100ns DRAMs and 12 MHz operation with 150ns DRAMs, 0 wait state 12MHz operation with 80ns DRAMs**
- **Separate CPU and AT Bus clocks**
- **Page Interleaved Memory supports single bank page mode, 2 way and 4 way page interleaved mode**
- **Integrated Lotus-Intel-Microsoft Expanded Memory Specification (LIM EMS) Memory Controller. Supports EMS 4.0.**
- **Software Configurable Command Delays, Wait states and Memory Organization**
- **Optimized for OS/2 operation**
- **Shadow RAM for BIOS and video ROM to improve system performance**
- **Complete AT/286 system board requires only 28 logic components plus memory and processor**
- **Targeted at Desktop PC/ATs, Laptops and CMOS Industrial Control Applications**
- **Available as four CMOS 84-pin PLCC or 100-pin PFP components.**

The CS8221 PC/AT compatible NEAT CHIPSet™ is an enhanced, high performance 4 chip VLSI implementation (including the 82C206 IPC) of the control logic used on the IBM™ Personal Computer AT. The flexible architecture of the NEAT CHIPSet™ allows it to be used in any 80286 based system.

The CS 8221 NEAT CHIPSet™ provides a complete 286 PC/AT compatible system,

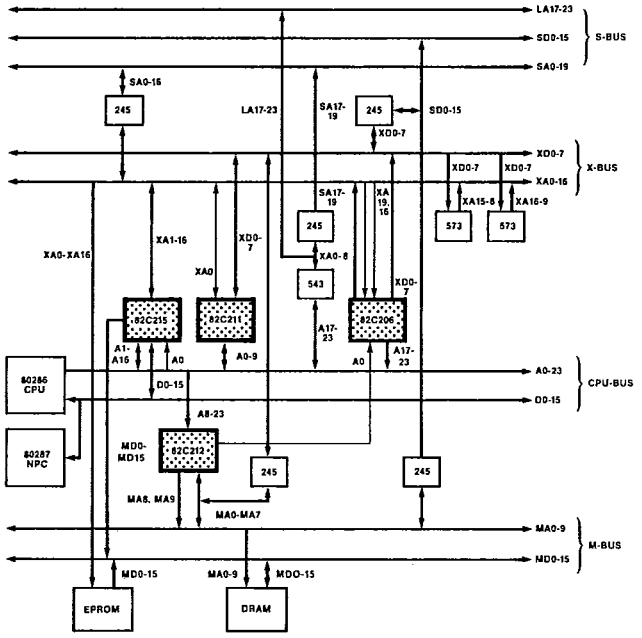


**Figure 1. NEAT System Block Diagram**

requiring only 24 logic components plus memory devices.

The CS8221 NEAT CHIPSet™ consists of the 82C211 CPU/Bus controller, the 82C212 Page/Interleave and EMS Memory controller, the 82C215 Data/Address buffer and the 82C206 Integrated Peripherals Controller (IPC).

The NEAT CHIPSet™ supports the local CPU bus, a 16 bit system memory bus, and the AT buses as shown in the NEAT System Block Diagram. The 82C211 provides synchronization and control signals for all buses. The 82C211 also provides an independent AT bus clock and allows for dynamic selection between the processor clock and the user selectable AT bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards.

The 82C212 Page/Interleave and EMS Memory controller provides an interleaved memory sub-system design with page mode operation. It supports up to 8 MB of on-board DRAM with combinations of 64Kbit, 256Kbit and 1Mbit DRAMs. The processor can operate at 16MHz with 0.5-0.7 wait state memory accesses, using 100 nsec DRAMs. This is possible through the Page Interleaved memory scheme. The Shadow RAM feature allows faster execution of code stored in EPROM, by down loading code from EPROM to RAM. The RAM then shadows the EPROM for further code execution. In a DOS environment, memory above 1Mb can be treated as LIM EMS memory.

The 82C215 Data/Address buffer provides the buffering and latching between the local CPU address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. The parity bit generation and error detection logic resides in the 82C215.

The 82C206 Integrated Peripherals Controller is an integral part of the NEAT CHIPSet™. It is described in the 82C206 Integrated Peripherals Controller data book.

### System Overview

The CS8221 NEAT CHIPSet™ is designed for use in 12 to 16 MHz 80286 based systems and provides complete support for the IBM PC/AT bus. There are four buses supported by the CS8221 NEAT CHIPSet™ as shown in Figure 1: CPU local bus (A and D), system memory bus (MA and MD), I/O channel bus (SA and SD), and X bus (XA and XD). The system memory bus is used to interface the CPU to the DRAMs and EPROMs controlled by the 82C212. The I/O channel bus refers to the bus supporting the AT bus adapters which could be either 8 bit or 16 bit devices. The X bus refers to the peripheral bus to which the 82C206 IPC and other peripherals are attached in an IBM PC/AT.

### Notation and Glossary

The following notations are used to refer to the configuration and diagnostics registers internal to the 82C211 and 82C212:

**REGnH** denotes the internal register of index n in hexadecimal notation.

**REGnH<x:y>** denotes the bit field from bits x to y of the internal register with index n in hexadecimal notation.

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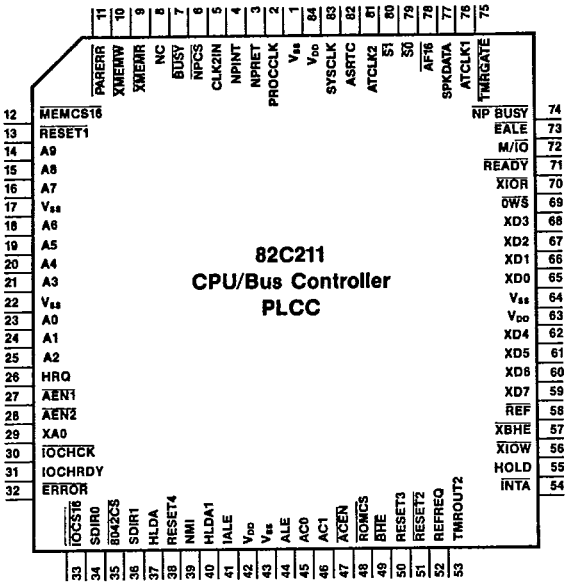
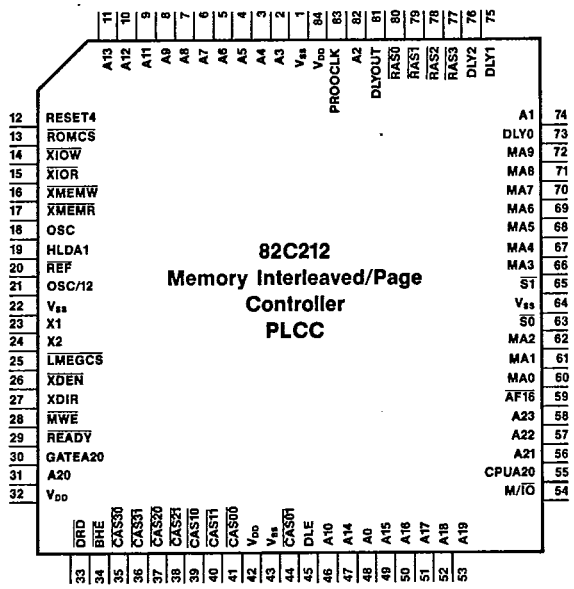

82C211
CPU/Bus Controller
PLCC
PARERR
XMEMW
XMEMR
NC
BUSY
NPCS
CLK2IN
NPINT
NPRET
PROCCLK
VSS
VDD
SYSCLK
ASRTC
ATCLK2
S1
S0
AF16
SPKDATA
ATCLK1
TMRGATE
MEMCS16
RESET1
A9
A8
A7
VSS
A6
A5
A4
A3
VSS
A0
A1
A2
HRQ
AEN1
AEN2
XA0
IOCHCK
IOCHRDY
ERROR
NP BUSY
EALE
M/IO
READY
XIOR
0WS
XD3
XD2
XD1
XD0
VSS
VDD
XD4
XD5
XD6
XD7
REF
XBHE
XIOW
HOLD
INTA
IOCS16
SDIR0
8042CS
SDIR1
HLDA
RESET4
NMI
HLDA1
IALE
VDD
VSS
ALE
AC0
AC1
ACEN
ROMCS
BHE
RESET3
RESET2
REFREQ
TMROUT2


82C212
Memory Interleaved/Page
Controller
PLCC
A13
A12
A11
A9
A8
A7
A6
A5
A4
A3
VSS
VDD
PROOCLK
A2
DLYOUT
RAS0
RAS1
RAS2
RAS3
DLY2
DLY1
RESET4
ROMCS
XIOW
XIOR
XMEMW
XMEMR
OSC
HLDA1
REF
OSC/12
VSS
X1
X2
LMEGCS
XDEN
XDIR
MWE
READY
GATEA20
A20
VDD
A1
DLY0
MA9
MA8
MA7
MA6
MA5
MA4
MA3
S1
VSS
S0
MA2
MA1
MA0
AF16
A23
A22
A21
CPUA20
M/IO
ORD
BHE
CAS30
CAS31
CAS20
CAS21
CAS10
CAS11
CAS00
VDD
VSS
CAS01
DLE
A10
A14
A0
A15
A16
A17
A18
A19

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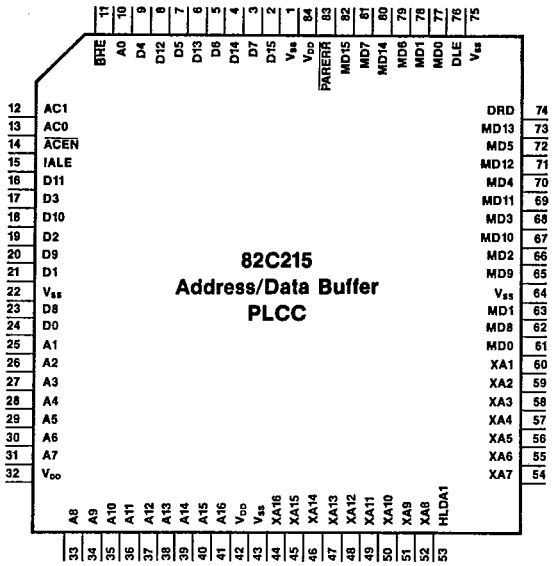
82C215
Address/Data Buffer
PLCC
1 BHE
2 A0
3 D4
4 D12
5 D5
6 D13
7 D6
8 D14
9 D7
10 D15
11 VSS
12 VDD
13 PARERR
14 MD15
15 MD7
16 MD14
17 MD6
18 MD1
19 MD0
20 DLE
21 VSS
22 DRD
23 MD13
24 MD5
25 MD12
26 MD4
27 MD11
28 MD3
29 MD10
30 MD2
31 MD9
32 VSS
33 MD1
34 MD8
35 MD0
36 XA1
37 XA2
38 XA3
39 XA4
40 XA5
41 XA6
42 XA7
43 A8
44 A9
45 A10
46 A11
47 A12
48 A13
49 A14
50 A15
51 A16
52 VDD
53 VSS
54 XA16
55 XA15
56 XA14
57 XA13
58 XA12
59 XA11
60 XA10
61 XA9
62 XA8
63 HLDA1
64 AC1
65 AC0
66 ACEN
67 IALE
68 D11
69 D3
70 D10
71 D2
72 D9
73 D1
74 VSS
75 D8
76 D0
77 A1
78 A2
79 A3
80 A4
81 A5
82 A6
83 A7
84 VDD

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## 82C211 Pin Description

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **Clocks** | | | |
| 5 | I | CLK2IN | CLOCK 2 input from a TTL crystal oscillator having a maximum of twice the rated frequency of the 80286 processor clock. |
| 2 | O | PROCCLK | PROCESSOR CLOCK output for the 80286 and the 82C212. It is derived from CLK2IN. It can also be programmed to be derived from ATCLK. |
| 76 | I | ATCLK1 | AT Bus Clock 1 input source from crystal or oscillator. This clock input is used for the AT bus operation and is only required if the AT bus state machine clock, BCLK (internal) will not be derived from CLK2IN. This clock input should be tied low if not used. Its frequency should be lower than CLK2IN. BCLK is the AT bus state machine clock and can be programmed to be equal to ATCLK. |
| 81 | O | ATCLK2 | AT Bus Clock 2 output is connected to the crystal (if a crystal is used to generate AT bus clock). A series damping resistor of 10 ohms should be used to reduce amplitude of the resonant circuit. It should be left open if a TTL oscillator is used. |
| 83 | O | SYSCLK | AT System Clock output is buffered to drive the SYSCLK line on the AT bus I/O channel. It is half the frequency of BCLK and should be between 6 and 8 MHz for maintaining correct AT I/O bus timing compatibility with the IBM™ PC/AT. |
| **Control** | | | |
| 13 | I | $\overline{\text{RESET1}}$ | RESET1 is an active low input generated by the power good signal of the power supply. When low, it activates RESET3 and RESET4. $\overline{\text{RESET1}}$ is latched internally. |
| 51 | I | $\overline{\text{RESET2}}$ | RESET2 is an active low input generated from the keyboard controller (8042/8742) for a "warm reset" not requiring the system power to be shut off. It forces a CPU reset by activating RESET3. |
| 38 | O | RESET4 | RESET4 is an active high output used to reset the AT bus, 82C206 IPC, 8042 keyboard controller, 82C212 memory controller. It is synchronized with the processor clock. |
| 50 | O | RESET3 | RESET3 is an active high output to the 80286 when $\overline{\text{RESET1}}$ or $\overline{\text{RESET2}}$ is active. It is also activated when shut-down condition in the CPU is detected. RESET3 will stay active for at least 16 PROCLK cycles. |

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**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **CPU Interface** | | | |
| 71 | I/O | $\overline{\text{READY}}$ | READY as an output, is driven low to terminate the current CPU cycle after IOCHRDY is high and $\overline{\text{0WS}}$ is high, or if "time out" condition is detected. During all other cycles, it is an input from the 82C212. It is an open collector output requiring an external pull-up resistor of 1KΩ and is connected to the 80286 $\overline{\text{READY}}$ pin. |
| 79, 80 | I | $\overline{\text{S0}}$, $\overline{\text{S1}}$ | STATUS is an active low input from the CPU. The status signals are used by the 82C211 to determine the state of the CPU. Pull up resistors of 10KΩ each should be provided. |
| 72 | I | M/$\overline{\text{IO}}$ | MEMORY INPUT/OUTPUT is the signal from the CPU. When high, it indicates a memory access, when low it indicates an I/O access. It is used to generate memory and I/O signals for the system. A 10KΩ pull up resistor is recommended. |
| 55 | O | HOLD | CPU HOLD REQUEST is an active high output to the CPU. It is activated during DMA, Master or refresh cycles. |
| 37 | I | HLDA | HOLD ACKNOWLEDGE is an active high input generated by the CPU to indicate to the requesting master that it has relinquished the bus. When active, it forces all commands ($\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{INTA}}$) to be tri-stated. |
| 49 | I/O | $\overline{\text{BHE}}$ | BYTE HIGH ENABLE is an active low signal which indicates the transfer of data on the upper byte of the data bus. In conjunction with A0, it is input during CPU cycles and in conjunction with XA0, it is output during DMA, MASTER cycles. A pull up resistor of 10KΩ is required. |
| 39 | O | NMI | NON MASKABLE INTERRUPT is an active high output to the NMI pin of the CPU and is generated by the 82C211 to invoke a non-maskable interrupt. |
| 41 | O | IALE | ADDRESS LATCH ENABLE (INTERNAL) is an active high output synchronized with PROCCLK and controls address latches used to hold addresses during bus cycles. It is not issued for halt bus cycles. |

**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **I/O Channel Interface** | | | |
| 31 | I | IOCHRDY | I/O CHANNEL READY is an active high input from the AT bus. When low it indicates a not ready condition and inserts wait states in AT-I/O or AT-memory cycles. When high it allows termination of the current AT-bus cycle. A series damping resistor of 53Ω at the AT bus connector is recommended to limit the negative under shoot. A 1KΩ pull up resistor is required for this open collector line. |
| 30 | I | $\overline{\text{IOCHCK}}$ | I/O CHANNEL CHECK is an active low input from the AT bus causing an NMI to be generated if enabled. It is used to signal an I/O error condition from a device residing on the AT bus. A 10KΩ pull up resistor is required. |
| 11 | I | $\overline{\text{PARERR}}$ | PARITY ERROR is an active low input from the 82C215 which causes an NMI if enabled. It indicates a parity error in local system memory. |
| 44 | O | ALE | ADDRESS LATCH ENABLE is an active high output to the AT bus and is synchronized with the AT state machine clock. It controls the address latches used to hold the addresses during bus cycles. This signal should be buffered to drive the AT bus. |
| 73 | O | $\overline{\text{EALE}}$ | EXTERNAL ADDRESS LATCH ENABLE is an active low output used to latch the CPU A17-A23 address lines to the LA17-LA23 lines on the AT bus. |
| **DMA Interface** | | | |
| 40 | O | HLDA1 | HOLD ACKNOWLEDGE 1 is an active high output when a bus cycle is granted in response to HOLD REQUEST 1. |
| 26 | I | HRQ | HOLD REQUEST is an active high input when DMA/Master is requesting a bus cycle. For an AT compatible architecture, it should be connected to the HOLD REQUEST signal from DMA1 and DMA2. |
| 27 | I | $\overline{\text{AEN1}}$ | ADDRESS ENABLE 1 is an active low input from one of the two DMA controllers enabling the address latches for 8 bit DMA transfers. |
| 28 | I | $\overline{\text{AEN2}}$ | ADDRESS ENABLE 2 is an active low input from one of the two DMA controllers enabling the address latches for 16 bit DMA transfers. |
| 48 | I | $\overline{\text{ROMCS}}$ | ROM CHIP-SELECT is an active low input from the 82C212. It is used to disable parity checks for local ROM cycles. |

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**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **Bus Inputs** | | | |
| 12 | I | $\overline{\text{MEMCS16}}$ | MEMORY CHIP SELECT 16 is an active low input from the AT bus indicating a 16 bit memory transfer. If high it implies an 8 bit memory transfer. A pull up resistor of 330Ω is required. |
| 33 | I | $\overline{\text{IOCS16}}$ | I/O CHANNEL SELECT 16 is an active low input from the AT bus indicating a 16 bit I/O transfer. If high it implies an 8 bit I/O transfer. A pull up resistor of 330Ω is required. |
| 69 | I | $\overline{\text{0WS}}$ | ZERO WAIT STATES is an active low input from the AT bus, causing immediate termination of the current AT bus cycle. Memories requiring zero wait states use this line to speed up memory cycles. It requires a 330Ω pull up resistor. |
| **Device Decode** | | | |
| 35 | O | $\overline{\text{8042CS}}$ | 8042 CHIP SELECT is an active low signal for the keyboard controller chip select. |
| 82 | O | ASRTC | ADDRESS STROBE to Real Time Clock is an active high signal used on the 82C206. |
| **Refresh** | | | |
| 52 | I | REFREQ | REFRESH REQUEST is an active high input initiating a DRAM refresh sequence. It is generated by the 8254 compatible timer controller #1 of the 82C206 IPC in a PC/AT implementation. |
| 58 | I/O | $\overline{\text{REF}}$ | REFRESH is an active low signal. As an open drain output, it initiates a refresh cycle for the DRAMs. As an input, it can be used to force a refresh cycle from an I/O device. An external pull up of 620Ω is required. |
| **X Bus Interface** | | | |
| 9 | I/O | $\overline{\text{XMEMR}}$ | X BUS MEMORY READ is an active low control strobe directing memory to place data on the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus. |
| 10 | I/O | $\overline{\text{XMEMW}}$ | X BUS MEMORY WRITE is an active low control strobe directing memory to accept data from the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus. |

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**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 70 | I/O | $\overline{\text{XIOR}}$ | X BUS I/O READ is an active low strobe directing an I/O port to place data on the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus. |
| 56 | I/O | $\overline{\text{XIOW}}$ | X BUS I/O WRITE is an active low strobe directing an I/O port to accept data from the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus. |
| 57 | I/O | $\overline{\text{XBHE}}$ | X BYTE HIGH ENABLE is an active low signal indicating the high byte has valid data on the bus. It is an output when the CPU is in control of the bus and is an input when a DMA controller is in control of the bus. A 4.7KΩ pull-up resistor is required on this line. |
| 59-62<br>65-68 | I/O<br>I/O | XD<7:4><br>XD<0:3> | X DATA BUS bits <7:0> |
| 8 | — | NC | No Connect |
| 75 | O | TMRGATE | TIMER GATE is an active high output that enables the timer on the 8254 compatible counter timer in the 82C206 to enable the tone signal for the speaker. |
| 53 | I | TMROUT2 | TIMER OUT 2 is an active high input from the 8254 compatible counter timer in the 82C206 that can be read from port B. |
| 77 | O | SPKDATA | SPEAKER DATA is an active high output used to gate the 8254 compatible tone signal of the 82C206 to the speaker. |
| 54 | O | $\overline{\text{INTA}}$ | INTERRUPT ACKNOWLEDGE is an active low output to the 82C206 interrupt controller. It is also used to direct data from the X to S bus during an interrupt acknowledge cycle. |
| **Buffer Control** | | | |
| 34 | O | SDIR0 | SYSTEM BUS DIRECTION 0 for the low byte. A low sets the data path from the S bus to the M bus. A high sets the data path from the M bus to the S bus. |
| 36 | O | SDIR1 | SYSTEM BUS DIRECTION 1 for the high byte. A low sets the data path from the S bus to the M bus. A high sets the data path from the M bus to the S bus |
| 47 | O | $\overline{\text{ACEN}}$ | ACTION CODE ENABLE is an active low output that validates the action code signals AC<1, 0> that are used by the 82C215 address/data buffer. |

**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 46, 45 | O | AC<1, 0> | ACTION CODE is a two bit encoded output command for bus size control and byte assembly operations performed in the 82C215. |
| **Memory Control** | | | |
| 78 | I | $\overline{AF16}$ | AF16 is an active low input indicating that the current cycle is a local bus cycle. A high indicates an AT bus cycle. A 10KΩ pull up resistor is required. |
| 23–25<br>18–21<br>14–18 | I/O | A<0:2><br>A<3:6><br>A<7:9> | ADDRESS lines A0–A9 are input from the CPU. These lines are output during refresh. A1 is used to detect shut down condition of the CPU. A0 is used to generate the enable signal for the data bus transceivers. |
| 29 | I/O | XA0 | ADDRESS line XA0 from the X bus. It is an output during CPU accesses on the X bus and is an input for 8 bit DMA cycles. |
| **CoProcessor Interface** | | | |
| 6 | O | $\overline{NPCS}$ | NUMERIC COPROCESSOR CHIP SELECT is an active low output signal used to select the internal registers of the 80287 NPX. |
| 7 | O | $\overline{BUSY}$ | BUSY is an active low output to the CPU initiated by the 80287 NPX, indicatig that it is busy. A 4.7KΩ pull up resistor is required. |
| 74 | I | $\overline{NPBUSY}$ | NUMERIC COPROCESSOR BUSY is an active low input from the NPX, indicating that it is currently executing a command. It is used to generate the BUSY signal to the CPU. A 4.7KΩ pull up resistor is required. |
| 32 | I | $\overline{ERROR}$ | ERROR is an active low input from the NPX indicating that an unmasked error condition exists. A 4.7KΩ pull up resistor is required. |
| 4 | O | NPINT | NUMERIC COPROCESSOR INTERRUPT is an active high output . It is an interrupt request from the 80287 and is connected to the IRQ13 line of the 82C206 IPC in a PC/AT environment. A 10KΩ pull up resistor is required. |

**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 3 | O | NPRESET | NUMERICAL PROCESSOR RESET is an active high reset to the 80287. It is active when RESET4 is active or when a write operation is made to Port 0F1H. In the later case, it is active for the period of the command. |
| **Power Supplies** | | | |
| 42, 63, 84 | — | VDD | POWER SUPPLY. |
| 1, 17, 22 43, 64 | — | VSS | GROUND. |

## 82C212 Pin Description

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **Clocks and Control** | | | |
| 83 | I | PROCCLK | PROCESSOR CLOCK input from the 82C211 |
| 23 | I | X1 | CRYSTAL 1 input from the 14.31818 MHz crystal. |
| 24 | O | X2 | CRYSTAL 2 output to the 14.31818 MHz crystal. |
| 18 | O | OSC | OSCILLATOR output for the system clock at 14.31818 MHz and has a drive capability of 24mA. |
| 21 | O | OSC/12 | OSCILLATOR divided by 12 is an output with a clock frequency equal to 1/12 of the crystal frequency across the X1, X2 pins. |
| 12 | I | RESET4 | RESET 4 is the active high reset input from the 82C211. It resets the configuration registers to their default values. When active, RAS<0:3> and CAS<00:31> remain high, OSC and OSC/12 remain inactive. |
| 20 | I | $\overline{REF}$ | REFRESH is an active low input for DRAM refresh control from the 82C211. It initiates a refresh cycle for the DRAMs. |
| 65, 63 | I | S<1, 0> | STATUS input lines from the CPU are active low. These lines are monitored to detect the start of a cycle. |
| 54 | I | M/$\overline{IO}$ | MEMORY I/O signal from the CPU. If high it indicates a memory cycle. If low, it indicates an I/O cycle. |
| 15 | I | $\overline{XIOR}$ | I/O READ command, input active low. |
| 14 | I | $\overline{XIOW}$ | I/O WRITE command, input active high. |
| 17 | I | $\overline{XMEMR}$ | X BUS MEMORY READ command, input active low. |
| 16 | I | $\overline{XMEMW}$ | X BUS MEMORY WRITE command, input active low. |
| 19 | I | HLDA1 | HOLD ACKNOWLEDGE 1 is an active high input from the 82C211. It is used to generate RAS and CAS signals for DMA cycles, in response to a hold request. |
| 13 | O | $\overline{ROMCS}$ | ROM CHIP SELECT is an active low chip select output to the BIOS EPROM. It can be connected to the output enable pin of the EPROM. |
| 48, 74, 82 | | A<0:2> | |
| 2-8 | | A<3:9> | |
| 46 | | A10 | |
| 9-11 | I | A<11:13> | ADDRESS input lines A<0:23> from the CPU local bus. |
| 47 | | A14 | |
| 49-53 | | A<15:19> | |
| 55-58 | | A<20:23> | |

**82C212 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 34 | I | $\overline{BHE}$ | BYTE HIGH ENABLE is an active low input from the CPU for transfer of data on the upper byte. |
| 29 | I/O | $\overline{READY}$ | READY is the system ready signal to the CPU. It is an active low output after requested memory or I/O data transfer is completed. It is an input when the current bus cycle is an AT bus cycle and is an output for local memory and I/O cycles. |
| 59 | O | $\overline{AF16}$ | AF16 is an active low output asserted on local memory (EPROM or DRAM) cycles. It is high for all other cycles. This signal is sampled by the 82C211. |
| **DRAM Interface** | | | |
| 77-80 | O | $\overline{RAS}$<3:0> | ROW ADDRESS STROBES 3 to 0 are active low outputs used as $\overline{RAS}$ signals to the DRAMs for selecting different banks. $\overline{RAS3}$ selects the highest bank and $\overline{RAS0}$ selects the lowest bank. These signals should be buffered and line terminated with 75Ω resistors to reduce ringing before driving the DRAM RAS lines. |
| 41 | O | $\overline{CAS00}$ | COLUMN ADDRESS STROBE 00 is an active low output used to select the low byte DRAMs of bank 0. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 44 | O | $\overline{CAS01}$ | COLUMN ADDRESS STROBE 01 is an active low output used to select the high byte DRAMs of bank 0. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 39 | O | $\overline{CAS10}$ | COLUMN ADDRESS STROBE 10 is an active low output used to select the low byte DRAMs of bank 1. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 40 | O | $\overline{CAS11}$ | COLUMN ADDRESS STROBE 11 is an active low output used to select the high byte DRAMs of bank 1. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 37 | O | $\overline{CAS20}$ | COLUMN ADDRESS STROBE 20 is an active low output used to select the low byte DRAMs of bank 2. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |

**82C212 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 38 | O | $\overline{\text{CAS21}}$ | COLUMN ADDRESS STROBE 21 is an active low output used to select the high byte DRAMs of bank 2. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 35 | O | $\overline{\text{CAS30}}$ | COLUMN ADDRESS STROBE 30 is an active low output used to select the low byte DRAMs of bank 3. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 36 | O | $\overline{\text{CAS31}}$ | COLUMN ADDRESS STROBE 31 is an active low output used to select the high byte DRAMs of bank 3. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 28 | O | $\overline{\text{MWE}}$ | MEMORY WRITE ENABLE is an active low output for DRAM write enable. |
| 45 | O | DLE | DATA LATCH ENABLE is an active high output used to enable the local memory data buffer latch in the 82C215. |
| 33 | O | $\overline{\text{DRD}}$ | DATA READ is an active low output used to transfer data from the memory bus to the local CPU bus in the 82C215. If high it sets the data path from the local CPU bus to the memory bus. |
| 81 | O | DLYOUT | DELAY LINE OUT is an active high output to the delay line for generating the DRAM control signals. |
| 73, 75, 76 | I | DLY<0:2> | DELAY IN 0, 1, 2 are active high inputs from the first to third taps on the delay line used to generate DRAM control signals. |
| 26 | O | $\overline{\text{XDEN}}$ | X DATA BUFFER ENABLE is an active low output asserted during I/O accesses to locations 22H and 23H. These locations contain the index and data registers for the NEAT CHIPSet™. It is used to enable the buffers between the XD and MA buses for accessing the 82C212 internal registers. |
| 27 | O | $\overline{\text{XDIR}}$ | X BUS DIRECTION is used to control the drivers between the X and S buses. The driver should be used such that data flow is from the S to X bus when $\overline{\text{XDIR}}$ is high and in the other direction when $\overline{\text{XDIR}}$ is low. |
| 71-72 | O | MA<8:9> | MULTIPLEXED DRAM ADDRESS lines MA8, MA9. These lines should be buffered and line terminated with 75Ω resistors before driving the DRAM address lines. |

**82C212 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 66-70<br>60-62 | I/O<br>I/O | MA<3:7><br>MA<0:2> | MULTIPLEXED DRAM ADDRESS lines MA0 to MA7. Also used as bi-directional lines to read/write to the internal registers of the 82C212. An external 74ALS245 buffer is required to isolate this path during normal DRAM operation. These lines should be buffered and line terminated with 75Ω resistors before driving the DRAM address lines. |
| **Miscellaneous** | | | |
| 31 | I/O | GA20 | ADDRESS line 20 is the gated A20 bit which is controlled by GATEA20. |
| 30 | I | GATEA20 | GATE ADDRESS 20 is an input used to force A20 low when GATEA20 is low. When high it propagates CPUA20 onto the A20 line. It is used to keep address under 1Mb during DOS operation. |
| 25 | O | $\overline{\text{LMEGCS}}$ | LOW MEG CHIP SELECT is an unlatched active low output asserted when the low Meg memory address space (0 to 1024 Kbytes) is accessed or during refresh cycles. It is used to disable $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$ signals on the AT bus if accesses are made beyond the 1Mbyte address space to maintain PC and PC/XT compatibility. |
| **Power and Ground** | | | |
| 32, 42, 84 | — | VDD | POWER SUPPLY. |
| 1, 22, 43, 64 | — | VSS | GROUND. |

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### 82C215 Pin Description

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **Controls** | | | |
| 14 | I | $\overline{\text{ACEN}}$ | ACTION CODE ENABLE is an active low input from the 82C211 that validates the action codes. |
| 12, 13 | I | AC<1:0> | ACTION CODES input from the 82C211 are used for bus sizing and byte assembly operations. They are discussed in Section 1.2.4. |
| 76 | I | DLE | DATA LATCH ENABLE is an active high input from the 82C212 used to enable the local memory data buffer latch. |
| 74 | I | $\overline{\text{DRD}}$ | DATA READ is an active low input from the 82C212 used to transfer data from the M data bus to the CPU data bus. If high, it sets the data path from the CPU data bus to the M data bus. |
| 53 | I | HLDA1 | HOLD ACKNOWLEDGE 1 is an active high input from the 82C211 used for address and data direction control during DMA cycles. |
| 15 | I | IALE | ADDRESS LATCH ENABLE (INTERNAL) is an active high input from the 82C211 used to latch the CPU address lines on to the X address lines. |
| 11 | I | $\overline{\text{BHE}}$ | BYTE HIGH ENABLE is an active low input from the CPU. It is used to enable the high byte parity checking. |
| 10 | I | A0 | ADDRESS line A0 is input from the CPU. It is used to enable the low byte parity checking. |
| **Address** | | | |
| 25-31<br>33-41 | I/O<br>I/O | A<1:7><br>A<8:16> | ADDRESS lines A1-A16 from the CPU. They are input during CPU and refresh cycles and output during DMA/ Master cycles. |
| 44-52<br>54-60 | I/O<br>I/O | XA<16:8><br>XA<7:1> | X ADDRESS lines XA16-XA1 (latched) are connected to the peripheral bus in the IBM™ PC/AT architecture. |
| **Data** | | | |
| 2, 4, 6, 8, 16, 18, 20, 23, 3, 5, 7, 9, 17, 19, 21, 24 | I/O | D<15:0> | DATA lines D15-D0 from the CPU. |

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**82C215 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 82, 80, 73, 71, 69, 67, 65, 62, 81, 79, 72, 70, 68, 66, 63, 61 | I/O | MD<15:0> | MEMORY DATA lines MD15-MD0 from the memory bus. |
| **Parity** | | | |
| 78, 77 | I/O | MP1, MP0 | MEMORY PARITY bits MP1, MP0 are the parity bits for the high and low order bytes of the system DRAMs. These lines are input during memory operations for parity error detection and are output during memory write operations for parity generation. |
| 83 | O | $\overline{\text{PARERR}}$ | PARITY ERROR is an active low output to the 82C211 which goes active upon detecting a parity error during a system memory read operation. It is used to generate a non-maskable interrupt to the CPU. |
| **Power and Ground** | | | |
| 32, 42, 84 | — | VDD | POWER |
| 1, 22, 43 64, 75 | — | VSS | GROUND |

# 1. 82C211 BUS CONTROLLER

## 1.1 Features

- Clock generation with software speed selection.
- Optional independent AT bus clock.
- CPU interface and bus control.
- Programmable command delays and wait state generation.
- Port B register.
- CPU state machine, AT bus state machine and bus arbitration logic
- Action Codes generation logic
- Port B register and NMI logic
- DMA and Refresh logic
- Numeric Coprocessor interface logic
- Configuration registers

## 1.2 Functional Description

The 82C211 Bus Controller consists of the following functional sub-modules as illustrated in figure 1.1:

- Reset and Shut down logic
- Clock generation and selection logic

### 1.2.1 Reset and Shut Down Logic

Two reset inputs $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ are provided on the 82C211 bus controller. $\overline{\text{RESET1}}$ is the Power Good signal from the power supply. When $\overline{\text{RESET1}}$ is active, the 82C211 asserts RESET3 and RESET4 for a system reset. $\overline{\text{RESET2}}$ is generated from the 8042 (or 8742) keyboard controller when a "warm reset" is required. The warm reset activates RESET3 to reset the 80286 CPU.

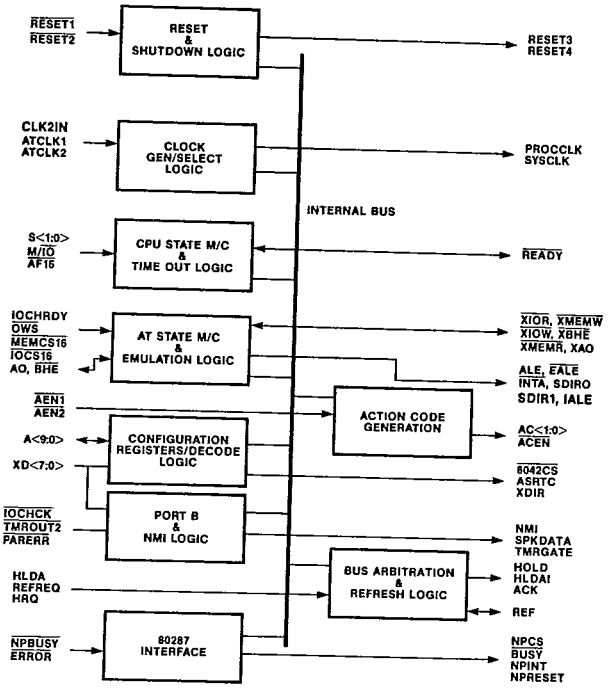


**Figure 1.1 82C211 Block Diagram**

RESET3 is also activated by the 82C211 when a shut down condition is detected in the CPU. Additionally, a low to high transition in REG60<5> causes RESET3 to be active after the current I/O command goes inactive. RESET3 is asserted for at least 16 PROCCLK cycles and then deasserted. RESET4 is used to reset the AT bus, 82C206 IPC, 8042 keyboard controller and the 82C212 memory controller. It is synchronized with respect to PROCCLK and is asserted as long as the Power Good signal is held low.

After a shut down condition is detected, RESET3 is asserted and held high for at least 16 PROCCLK cycles and then deasserted. RESET3 resulting from a shut down condition is synchronous with PROCCLK, ensuring proper CPU operation. Both RESET3 and RESET4 meet the setup and hold timing requirements of the 80286 CPU.

### 1.2.2 Clock Generation and Selection Logic

The 82C211 provides a flexible clock selection scheme as shown in Figure 1.2. It has two input clocks; CLK2IN and ATCLK. CLK2IN is driven from a TTL crystal oscillator, running at a maximum of twice the processor clock (PROCCLK) frequency. ATCLK is derived from a crystal. Typically, it should be of a lower frequency than CLK2IN. ATCLK and CLK2IN can be selected under program control.

The 82C211 generates processor clock, PROCCLK, for driving the CPU state machine and interface. SCLK (internal) is PROCCLK/2 and is in phase with the internal states of the 80286. BCLK (internal) is the AT bus state machine clock and is used for the AT bus interface. SYSCLK is the AT bus system clock and is always BCLK/2.

PROCCLK can be derived from CLK2IN or from ATCLK. In the synchronous mode, both PROCCLK and BCLK are derived from CLK2IN, so that the processor state machine and the AT bus state machine run synchronous. In the asynchronous mode, BCLK is generated from the ATCLK and PROCCLK is generated from CLK2IN or the ATCLK. In this case, the processor and AT bus state machines run asynchronous to each other. The following clock selections are possible:

**Synchronous mode**

1. PROCCLK = BCLK = CLK2IN
   SYSCLK = BCLK/2 = CLK2IN/2
2. PROCCLK = CLK2IN
   BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4
3. PROCCLK = BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4

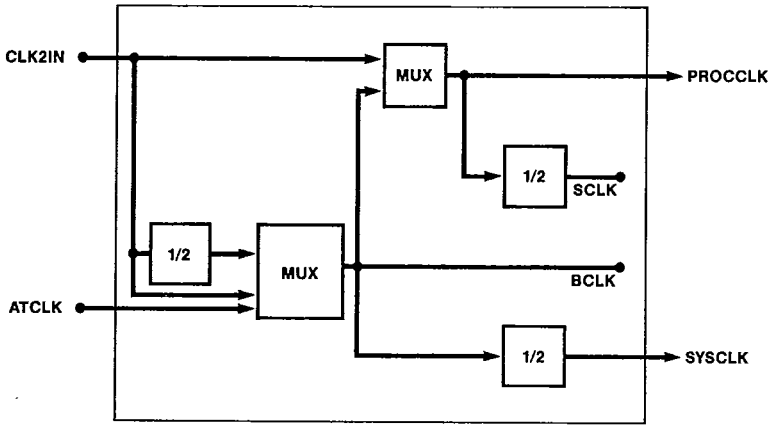


**Figure 1.2 Clock Selection Block Diagram**

**Asynchronous mode**

1. PROCCLK = CLK2IN
   BCLK = ATCLK
   SYSCLK = BCLK/2 = ATCLK/2
2. PROCCLK = ATCLK
   BCLK = ATCLK
   SYSCLK = BCLK/2 = ATCLK/2.

Under normal operation, CLK2IN should be selected as the processor clock (PROCCLK) to allow the processor to run at full speed. BCLK can either be a sub-division of CLK2IN or the ATCLK. ATCLK may be selected to generate PROCCLK only when it is desired to slow down the processor for timing dependent code execution. Once the options for clock switching are set, the switching occurs with clean transition in the asynchronous or synchronous mode. During clock switching, no phases of PROCCLK are less than the minimum value or greater than the maximum value specified for the 80286 CPU. The clock source selection is made by writing to REG62H<0:1> first and then to REG60H<4>, which default to: PROCCLK = CLK2IN, SYSCLK = CLK2IN/4.

Figures 1.3 and 1.4 illustrate the sequence of events that switch PROCCLK from high to low speed and from low to high speed, upon receiving a request from the configuration register. In Figure 1.3, the falling edge (A) of PROCCLK is used to latch the command inactive condition (1). On the falling edge (B), CLK2IN is disabled on the PROCCLK line. This ensures that clock switching will occur when PROCCLK is low. Once CLK2IN has been disabled, the first rising edge (C) of BCLK latches this condition as denoted by sequence (2). BCLK then enables itself on the PROCCLK line on the falling edge (D) as

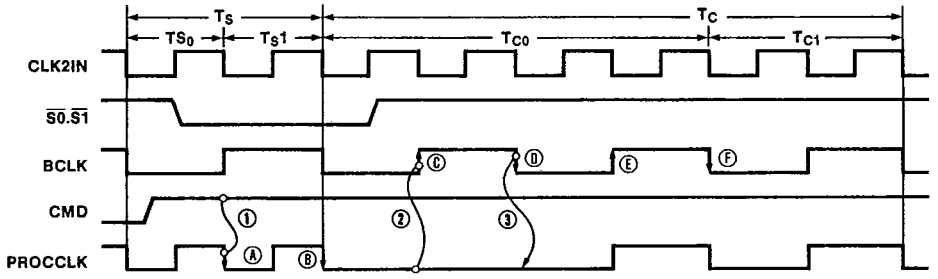


**Figure 1.3 Sequence Diagram for High to Low Frequency Transition**

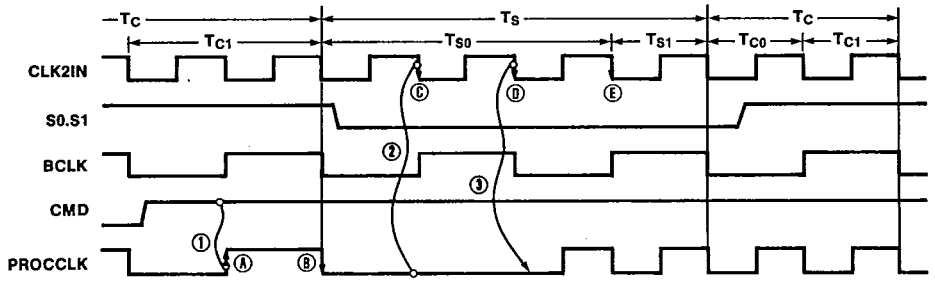


**Figure 1.4 Sequence Diagram for Low to High Frequency Transition**

denoted by sequence (3). This ensures a glitch free transition between the two clocks. It also does not violate the min and max 80286 CPU clock specifications. If BCLK is asynchronous with respect to CLK2IN, it is possible that sequence (2) could violate setup time requirements with respect to edge (C). In this case, edge (D) will register the state of PROCCLK as still being high in sequence (3). Hence, edge (E) samples PROCCLK to be low and edge (F) enables BCLK on the PROCCLK line. This case does not violate the min and max 80286 CPU clock specifications.

In Figure 1.4, the rising edge (A) of PROCCLK latches command inactive as denoted by sequence (1). Edge (B) disables BCLK on the PROCCLK line. In sequence (2), edge (C) of CLK2IN latches PROCCLK low. Edge (D) then enables CLK2IN on the PROCCLK line as denoted by sequence (3). If sequence (2) does not meet setup time requirements of edge (C), then the state of PROCCLK is sampled as being high in sequence (2). In this case, edge (D) samples PROCCLK low and edge (E) enables CLK2IN on the PROCCLK line. In this case also, PROCCLK does not violate the min and max 80286 CPU clock specifications.

### 1.2.3 CPU State Machine, Bus State Machine and Bus Arbitration

In order to extract maximum performance out of the 80286 on the system board, it is desirable to run the system board at the rated maximum CPU frequency. This frequency may be too fast for the slow AT bus. In order to overcome this problem, the 82C211 has two state machines: the CPU state machine which typically runs off CLK2IN, and the AT bus state machine which runs off BCLK. The two state machines maintain an asynchronous protocol under external mode operation.

#### CPU State Machine

Interface to the 80286 requires interpretation of the status lines $\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$ during TS0 and the synchronization and generation of $\overline{READY}$ to the CPU upon completion of the requested operation. $\overline{ALE}$ is issued in response to the beginning of a new cycle in TS1 by the 82C211. If $\overline{AF16}$ is detected as being inactive at the end of the processor TS state, control is handed over to the AT bus state machine. The CPU state machine then waits for $\overline{READY}$ to be active to terminate the current cycle. All local memory cycles are 16 bit cycles. If $\overline{AF16}$ is asserted in response to a new CPU cycle and READY is not returned to the 82C211 within 128 clocks, and REG60H<2> is enabled, then an NMI is generated to signal bus time-out, if NMI has been enabled.

#### AT Bus State Machine

The AT bus state machine gains control when $\overline{AF16}$ is detected inactive by the CPU state machine. It uses BCLK which is twice the frequency of AT system clock SYSCLK. When ATCLK is selected as the source for BCLK, it also performs the necessary synchronization of control and status signals between the AT bus and the processor. The 82C211 supports 8 and 16 bit transfers between the processor and 8 or 16 bit memory or I/O devices located on the AT bus. The action codes AC0, AC1 qualified by $\overline{ACEN}$ are used for bus sizing and 8, 16 bit bus conversions by the 82C215. They are discussed in section 1.2.4.

The AT bus cycle is initiated by asserting ALE in AT-TS1. On the falling edge of ALE, $\overline{MEMCS16}$ is sampled for a memory cycle to determine the bus size. It then enters the command cycle AT-TC and provides the sequencing and timing signals for the AT bus cycle. For an I/O cycle, $\overline{IOCS16}$ is sampled in the middle of the processor TC state. These control signals emulate the lower speed AT bus signals. The command cycle is terminated when IOCHRDY is active on the AT bus and all programmed wait states have been executed.

It is possible to provide software selectable wait states and command delays to the AT state machine. Providing command delays causes the commands ($\overline{XMEMR}$, $\overline{XMEMW}$, $\overline{XIOR}$ or $\overline{XIOW}$)to be delayed from going active in BCLK steps. Providing wait states causes READY to be delayed to the CPU in steps of the AT command cycles (AT-TC). The defaults and settings are discussed in section 1.4.

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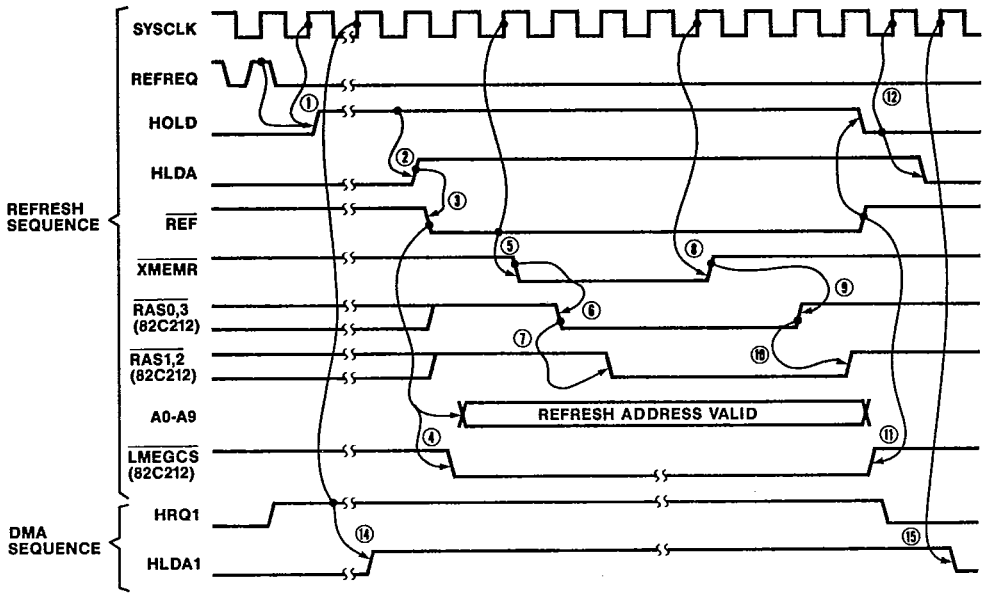



**Figure 1.5 Refresh/DMA Sequence**

### Bus Arbitration

The 82C211 controls all bus activity and provides arbitration between the CPU, DMA/Master devices, and DRAM refresh logic. It handles HRQ and REFREQ by generating HOLD request to the CPU and arbitrating among these requests in a non-preemptive manner. The CPU relinquishes the bus by issuing HLDA. The 82C211 responds by issuing $\overline{REF}$ or HLDA1 depending on the requesting device. During a refresh cycle, the refresh logic has control of the bus until $\overline{REF}$ goes inactive. $\overline{XMEMR}$ is asserted low during a refresh cycle and the refresh address is provided on the A0-A9 address lines by the 82C211 to be used by the 82C212 memory controller. During a DMA cycle, the DMA controller has control of the bus until HRQ goes inactive. The 82C211 puts out the action codes for bus sizing. ALE, $\overline{EALE}$ and $\overline{ACEN}$ are active during DMA cycle.

Figure 1.5 is a sequence diagram for Refresh/DMA cycles. Upon receiving a refresh request (REFREQ) it is internally latched by the 82C211. On the first rising edge of SYSCLK, HOLD is output to the processor in sequence 1. Depending on the current activity of the processor, a hold acknowledge (HLDA) is issued by the processor in sequence 2, after a DMA latency time. The 82C211 responds with $\overline{REF}$ active in sequence 3. $\overline{LMEGCS}$ from the 82C212 goes active in sequence 4. $\overline{XMEMR}$ is asserted low on the second rising edge of SYSCLK after $\overline{REF}$ is low in sequence 5. The 82C212 pulls all its RAS lines ($\overline{RAS0}$-$\overline{RAS3}$) high when $\overline{REF}$ goes low. The RAS lines go active in sequences 6 and 7 when the refresh address is active on the A0-A9 lines of the 82C211. The 82C212 uses the A0-A9 lines to generate the refresh address on the MA0-MA9 address lines. $\overline{XMEMR}$ goes inactive in sequence 8 followed by the RAS lines going inactive in sequences 9, 10. $\overline{REF}$, $\overline{LMEGCS}$ and HOLD go inactive in sequence 11. Control is transferred to the CPU after HLDA goes inactive in sequence 12.

If a DMA device requests control of the bus,

the 82C211 receives HRQ1 active. After a DMA latency time, the CPU relinquishes the bus to the requesting device by issuing HLDA1 in sequence 14. HLDA1 is active as long as HRQ1 is active. Once the DMA device de-asserts HRQ1, HLDA1 is deasserted by the 82C211 in sequence 15, to return control to the processor.

### 1.2.4 Action Codes Generation Logic

The AT state machine performs data conversion for CPU accesses to devices not on the CPU or Memory Bus.The AT bus conversions are performed for 16 to 8 bit read or write operations. Sixteen bit transfers to/from the CPU are broken into smaller 8 bit AT bus or peripheral bus reads or writes. The action codes are generated as shown in Table 1.1 to control the buffers in the 82C215. The action codes are in response to signals $\overline{\text{MEMCS16}}$, $\overline{\text{IOCS16}}$.

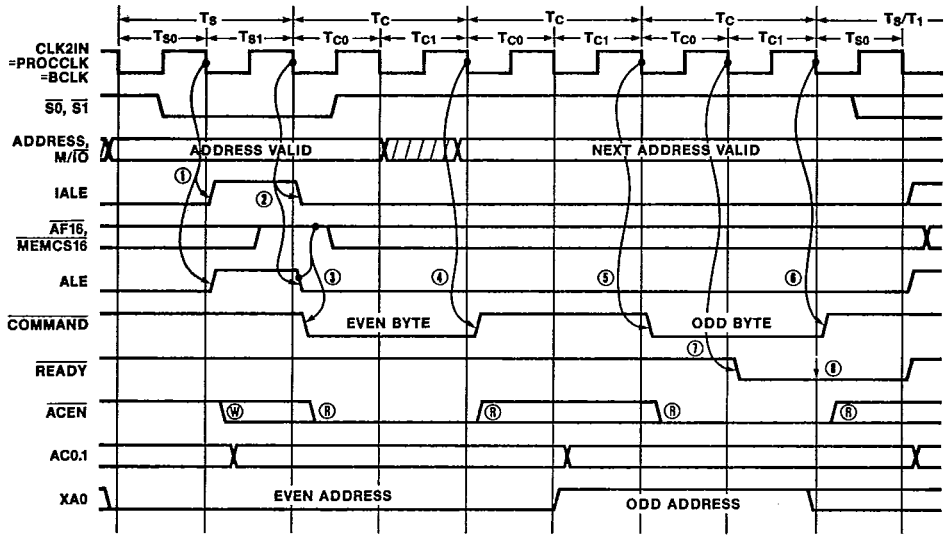
**Table 1.1**

**Action Codes Enable ($\overline{\text{ACEN}}$) Generation**

| Operation | $\overline{\text{ACEN}}$ |
|---|---|
| DMA/MASTER | 0 |
| CPU (local) | 1 |
| CPU (AT bus) | 0 for write<br>0 qualified by command for read and interrupt acknowledge cycles |
| REFRESH | 1 qualified by REF |

**AT-Bus CPU Cycles HLDA1 = 0**

| AC | Operation |
|---|---|
| 00 | 16 bit write and 8 bit write (low byte) |
| 01 | 16 bit read and 8 bit read (low byte) |
| 10 | 8 bit write (high byte) |
| 11 | 8 bit read (high byte) |




NOTE: W.S. = WAIT STATUS, C.D. = COMMAND DELAYS, R = READ CYCLE, W = WRITE CYCLE.

**Figure 1.6 Quick Mode Bus Conversion Cycle (0WS, 0CD)**

**DMA/MASTER Cycles, HLDA1 = 1**

| AC | Operation |
|---|---|
| 00 | MD bus tri-stated from the 82C215 for 16 bit and 8 (low byte) read/write operations |
| 01 | Reserved |
| 10 | High memory write MD0-7 to MD8-15 |
| 11 | High memory read MD8-15 to MD0-7 |

Figure 1.6 shows a sequence diagram for a data conversion cycle in Quick mode with zero wait states (0 W.S.) and zero command delays (0 C.D.). Quick mode is discussed in section 1.3.2. In Quick mode ALE is issued on the AT bus as shown in sequences 1 and 2. MEMCS16 from an external device is sampled high by the 82C211 in sequence 3, initiating a bus conversion cycle. The first command also goes active in sequence 3 for the first byte operation and is terminated in sequence 4. In order to provide sufficient back to back time between the two 8 bit cycles, the second byte command is issued two PROCCLKs later in sequence 5 and is terminated in sequence 6. No second ALE is issued for the second byte operation since only address line XA0 changes from zero to one. READY is asserted low in sequence 7 and is sampled low by the processor in sequence 8, to terminate the current cycle. ACEN and AC0, AC1 are issued by the 82C211 for bus conversion as shown.

### 1.2.5 Port B and NMI generation logic

The 82C211 provides access to Port B defined for the PC/AT as shown in Figure 1.7.

| IO ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| 61H | PCK | CHK | T20 | RFD | EIC | EPR | SPK | T2G | PORT B |

**Figure 1.7 Port B**

| Bits | Read/ Write | Function |
|---|---|---|
| 7 | R | PCK-System memory parity check |
| 6 | R | CHK-I/O channel check |
| 5 | R | T20-Timer 2 Out |
| 4 | R | RFD-Refresh Detect |
| 3 | R/W | EIC-Enable I/O channel check |
| 2 | R/W | ERP-Enable system memory parity check |
| 1 | R/W | SPK-Speaker Data |
| 0 | R/W | T2G-Timer 2 Gate (Speaker) |

**Table 1.2 Port B register definition**

The NMI sub-module performs the latching and enabling of I/O and parity error conditions, which will generate a non-maskable interrupt to the CPU if NMI is enabled. Reading Port B will indicate the source of the error condition (IOCK and PCHK). Enabling and disabling of NMI is accomplished by writing to I/O address 070H. On the rising edge of XIOW, NMI will be enabled if data bit 7 (XD7) is equal to 0 and will be disabled if XD7 is equal to 1.

### Numeric Coprocessor Interface

Incorporated in the 82C211 is the circuitary to interface an 80287 Numeric Coprocessor to 80286. The circuitary handles the decoding required for selecting and resetting the Numeric Coprocessor, handling NPBUSY and ERROR signals from the 80287 to the CPU, and generating interrupt signals for error handling.

The NPCS signal is active for I/O addresses 0F8H-0FFH, used to access the internal registers of the 80287. It is also active for I/O addresses 070H-NMI mask register, 0F0H-Clear Numeric Coprocessor BUSY signal, and 0F1H-Clear the Numerical Coprocessor and Numerical Coprocessor BUSY signal. While executing a task, the 80287 issues an NPBUSY

signal to the 82C211. Under normal operation, it is passed out to the CPU as $\overline{BUSY}$. If during this busy period, a numeric coprocessor error occurs, $\overline{ERROR}$ input to the 82C211 becomes active, resulting in latching of the BUSY* output and assertion of NPINT. Both signals stay active until cleared by an I/O write cycle to address 0F0H or 0F1H. A system reset clears both NPINT and $\overline{BUSY}$ latches in the 82C211. The 80287 is reset through the NPRESET output, which can be activated by a system reset or by performing a write operation to I/O port 0F1H.

### 1.3 Modes of Operation of the 82C211

The 82C211 has 4 modes of operation for different CPU and AT bus clock selections:

Normal mode
Quick mode
Delayed mode
External mode

#### 1.3.1 Normal mode

This mode is enabled by default (without writing to the internal registers of the 82C211). Under Normal mode:

PROCCLK = CLK2IN
BCLK = CLK2IN/2
SYSCLK = CLK2IN/4

Since the CPU state machine clock and the AT bus state machine clock are derived from CLK2IN, this is a synchronous mode. ALE and commands ($\overline{XMEMR}$, $\overline{XMEMW}$, $\overline{XIOR}$, $\overline{XIOW}$) are issued only for AT bus cycles and not for local cycles. If activated by default, I/O cycles will have one command delay, 8 bit AT memory cycles will have 4 wait states, 16 bit AT memory cycles will have 1 wait state.

Figure 1.8 shows the sequence diagram of a Normal mode local cycle followed by an AT bus cycle with zero wait states (0 W.S.) and

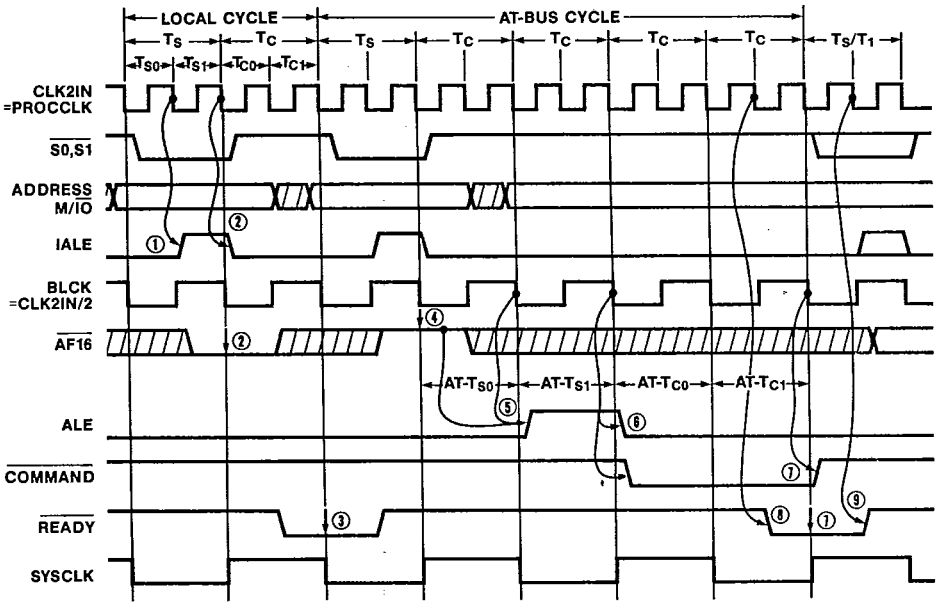
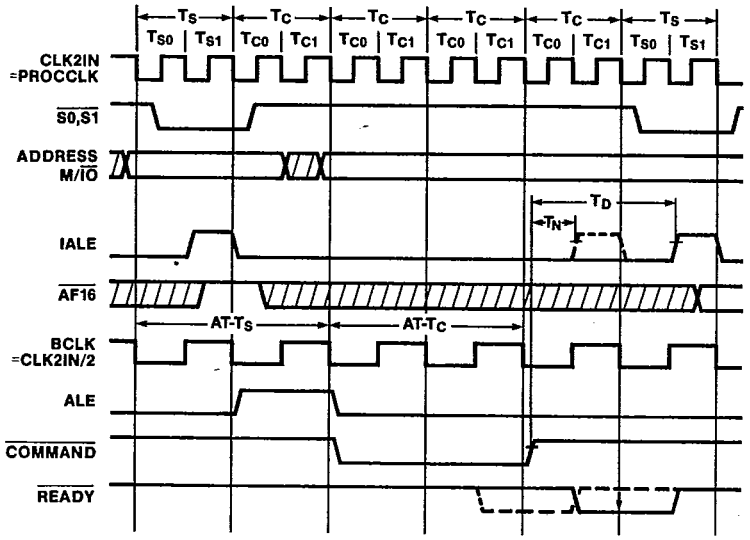



**Figure 1.8 Normal Mode Local Cycle Followed by AT Bus Cycle (0WS, 0CD)**




NOTE: TD = DELAYED HOLD TIME, TN = NORMAL HOLD TIME.

**Figure 1.9 Normal Mode AT Bus Cycle with Additional Hold Time (0WS, 0CD)**

zero command delays (0 C.D.). In sequences 1 and 2, IALE is generated from CLK2IN. AF16 is sampled to be low in sequence 2. ALE and AT buss commands (XIOR, XIOW, XMEMR, MEMW) are not generated since it is a local cycle. For a zero wait state cycle, ready is sampled low by the 80286 CPU in sequence 3 and the cycle is terminated. For the AT bus cycle, AF16 is sampled high in sequence 4. Control is transferred to the AT bus state machine. BCLK then generates the AT bus states. ALE is generated in sequences 5 and 6. The AT bus command is generated in sequences 6 and 7, for zero command delays programmed in the 82C211. For a zero wait state cycle, ready is asserted low as shown in sequences 8 and 9, to be sampled by the CPU in sequence 7. This terminates the AT bus cycle.

On the AT bus, certain slow peripherals require between 50 to 60 nanoseconds between command going inactive to the next ALE going active, to provide sufficient data recovery time. The sequence diagram in Figure 1.9 shows a Normal mode AT bus cycle with additional hold time. The dotted IALE signal would have been valid, if the additional hold time register had not been enabled in RA1<7>. Instead, IALE is delayed by one $T_C$ state of the processor by asserting READY one $T_C$ cycle later. The 82C212 provides an extended DLE to the 82C215 in this mode, so that data is available to the CPU during write cycles. If this mode was not invoked, then READY would have been asserted earlier as shown by the dotted line. In Delayed mode, the 82C211 provides an extended data hold time. This additional hold time can only be programmed in the Normal mode.

### 1.3.2 Quick mode

This mode is also a synchronous mode and is enabled by writing a zero to REG61<6> and the following clock selections have been made:

PROCCLK = BCLK = CLK2IN
SYSCLK = CLK2IN/2

In Quick mode, an ALE signal is generated

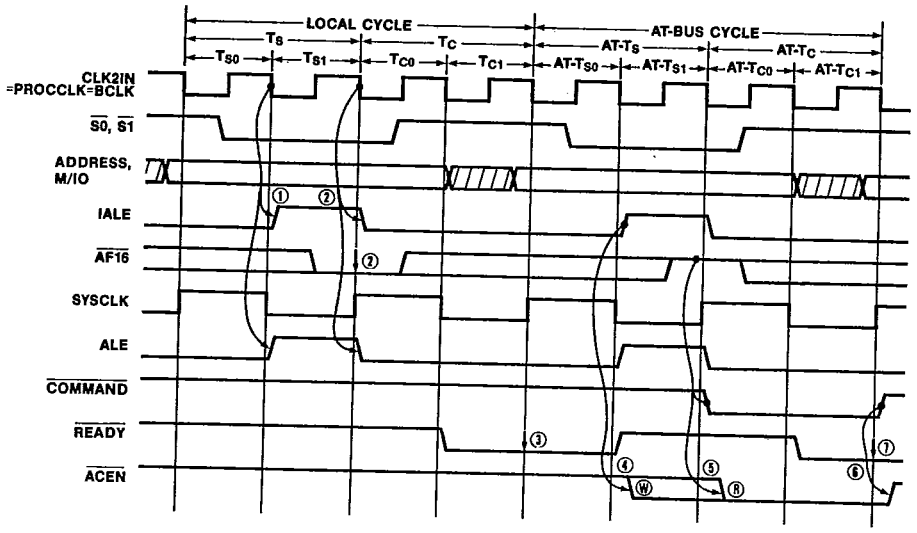



**Figure 1.10 Quick Mode Local Cycle Followed by AT Bus Cycle (0WS, 0CD)**

on the AT bus for both AT bus and local bus cycles. However, the commands (XMEMR, XMEMW, XIOR, XIOW) are not issued for local bus cycles.

The sequence diagram for a Quick mode local cycle followed by an AT bus cycle is shown in Figure 1.10. In this mode, both IALE and ALE are generated in sequences 1 and 2 for the local cycle. Hence, an ALE is issued on the AT bus for AT or non-AT bus cycles. The local cycle is terminated when READY is sampled low by the 80286 in sequence 3. For the AT bus cycle, the command is issued after AF16 is sampled high in sequence 5. For write cycles, ACEN is activated in sequence 4. For read cycles, ACEN is activated in sequence 5. If the next cycle is not an AT bus write cycle, then ACEN is negated in sequence 6. READY is sampled low by the 80286 in sequence 6, to terminate the cycle. As seen in Figure 1.10, the AT bus states coincide with the CPU states for AT bus cycles. Hence, Quick mode is performance efficient when switching between local and AT bus cycles. This mode is useful for high speed add-on cards such as Lazer Printer interface cards.

### 1.3.3 Delayed mode

This mode is another synchronous mode and is enabled when Quick mode is disabled and the following clock selections have been chosen made:

PROCCLK = CLK2IN
BCLK = CLK2IN
SYSCLK = CLK2IN/2

In Delayed mode, ALE and commands are issued only for AT bus cycles like in the Normal mode, except that BCLK = CLK2IN. ALE and commands are not issued for local cycles. Figure 1.11 shows a Delayed mode AT bus cycle. IALE is generated in sequences 1 and 2. ALE is asserted in sequence 3 after sampling AF16 high and it is deasserted in sequence 4. Hence the AT bus states, though synchronous, are delayed with respect to the processor states. Figure 1.11 is an example with two command delays and three wait states. The dotted lines A and B show command going active for 0 and 1 command delays. Sequence 5 shows command going active for programmed 2 command delays.

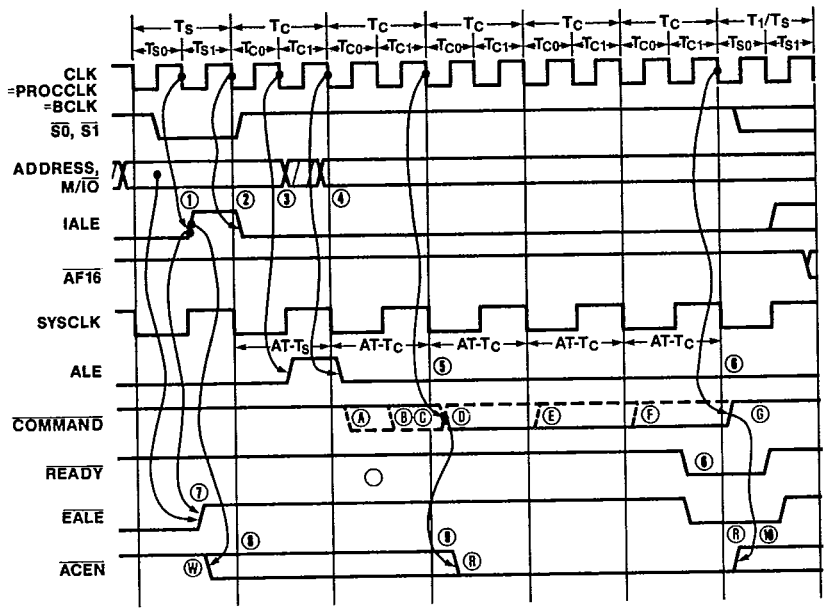



**Figure 1.11 Delayed Mode AT Bus Cycle (3WS, 2CD)**

Dotted lines D, E, F show command going inactive for 0, 1, 2 wait states. Sequence 6 shows command going inactive for programmed 3 wait states. READY is sampled by the 80286 in sequence 6 to terminate the current cycle. Since the AT bus states are delayed with respect to the processor states, the Local Address lines LA17-LA23 (typically un-latched) are not valid when ALE is active. In order to have the LA17-LA23 lines valid when ALE is active, they are latched by EALE as shown in sequence 7. Sequences 8, 9 show when ACEN is asserted for AT bus write (W) and read (R) cycles. ACEN is deasserted in sequence 10. This mode is useful for slow peripheral AT add-on cards.

### 1.3.4 External mode

This is an asynchronous mode and is enabled when ATCLK is selected as the source for BCLK. The following clock selections are required in this mode:

PROCCLK = CLK2IN
BCLK = ATCLK
SYSCLK = ATCLK/2

Since ATCLK is asynchronous to CLK2IN, the CPU state machine runs asynchronous to the AT bus state machine. ALE and commands (XMEMR, XMEMW, XIOR, XIOW) are issued only for AT bus cycles. These signals are inactive for local cycles. Figure 1.12 shows a sequence diagram for an External mode AT bus cycle. AF16 is sampled high in sequence 2 and is latched internally, using CLK2IN. The asynchronous BCLK samples this latched state on the next rising edge of BCLK. In the example shown, edge A samples the latched AF16 signal (internal) high. This causes the AT state machine to issue an ALE in sequences 3 and 4. For a zero command delay, zero wait states cycle, the command is issued on the AT bus in sequences 4 and 6, synchronized with BCLK. For write cycles, ACEN is asserted in sequence 1 and for read cycles, it is asserted in sequence 5. ACEN is deasserted in sequence 7. The command inactive state is sampled by CLK2IN on every rising edge. In this case, edge D of CLK2IN samples command high (sequence 8). It is followed by the assertion of READY in sequence 9, syn-

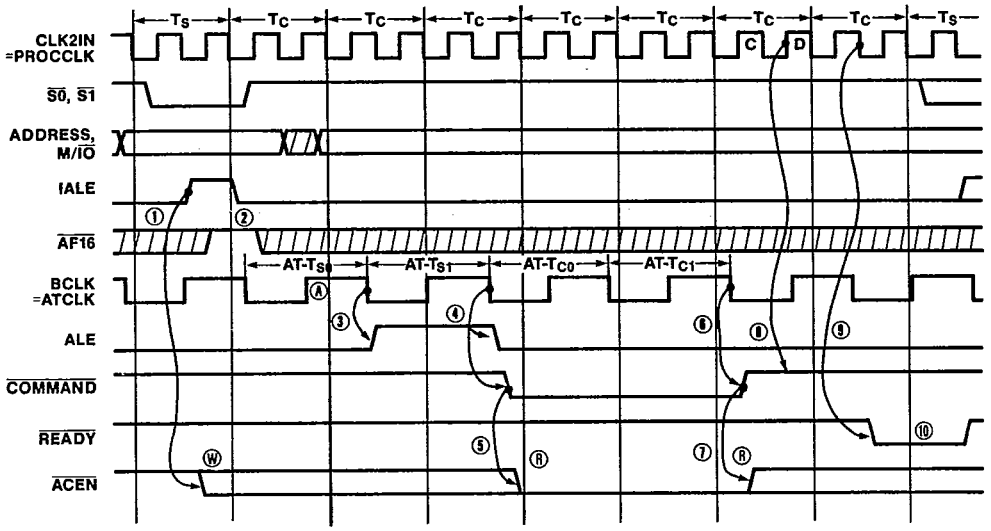



**Figure 1.12 External Mode AT Bus Cycle (0WS, 0CD)**

chronized with CLK2IN. The CPU samples READY low in sequence 10 and terminates the current cycle.

### 1.4 Configuration Registers

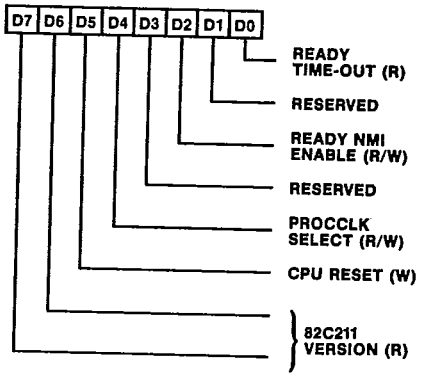
There are three bytes of configuration registers in the 82C211; RA0, RA1 and RA2. An indexing scheme is used to reduce the I/O ports required to access all the registers required for the NEAT CHIPSet. Port 22H is used as an indexing register and Port 23H is used as the data register. The index value is placed in port 22H to access a particular register and the data to be read from or written to that register is located in port 23H. Every access to port 23H must be preceded by a write of the index value to port 22H even if the same register data is being accessed again. All reserved bits are set to zero by default and when written to, must be set to zero. Table 1.3 lists the three registers:

**Table 1.3**

| Register Number | Register Name | Index |
|---|---|---|
| RA0 | PROCCLK Selector | 60H |
| RA1 | Command Delay | 61H |
| RA2 | Wait State/ BCLK Selector | 62H |

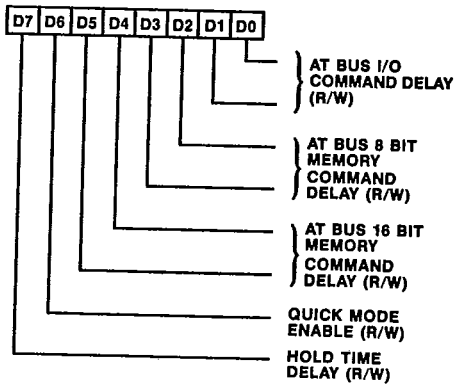
### 1.4.1 Register Description

**PROCCLK Register RA0**
Index register port: 22H
Data register port: 23H
Index: 60H




| Bits | Function |
|---|---|
| 7, 6 | 82C211 revision number. 00 is the initial number. |
| 5 | Alternate CPU reset. A low to high transition in this bit activates a CPU reset. Once active, it remains active for 16 PROCCLK cycles and then goes low. |
| 4 | Processor clock select is by default set to zero and selects PROCCLK = CLK2IN. If high, it selects PROCCLK = BCLK. |
| 3 | Reserved.* |
| 2 | Local bus READY timeout NMI enable. A one enables the NMI and a zero disables it. Default is 0 |
| 1 | Reserved.* |
| 0 | Local bus READY timeout. A one indicates that READY timeout has occurred 128 PROCCLK cycles after $\overline{AF16}$ has been asserted. A zero indicates that READY time out has not occurred. |

**Command Delay Register RA1**
Index register port: 22H
Data register port: 23H
Index: 61H




| Bits | Function |
|---|---|
| 1, 0 | AT Bus I/O cycle command delay. Specifies between 0 to 3 BCLK cycle command delays for AT I/O cycles. Default is 1. |
| 3, 2 | AT Bus 8 bit memory command delay. Specifies between 0 to 3 BCLK cycle command delays for 8 bit AT memory cycles. Default is 1. |
| 5, 4 | AT Bus 16 bit memory command delay. Specifies between 0 and 3 BCLK cycle command delays for 16 bit AT memory cycles. Default is 0 |
| 6 | Quick mode enable. A zero enables Quick mode and a one disables it. Default is 1. |
| 7 | Address hold time delay. A one enables extra address bus hold time and a zero disables it. Default is 0. |

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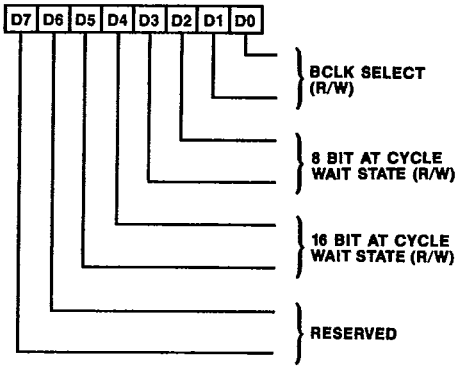
**Wait States Register RA2**
Index register port: 22H
Data register port: 23H
Index: 62H




| Bits | Function |
|---|---|
| 1, 0 | Bus clock (BCLK) source select. Default is 00. |
| 00 | BCLK = CLK2IN/2 |
| 01 | BCLK = CLK2IN |
| 10 | BCLK = ATCLK |
| 11 | Reserved |
| 3, 2 | 8 bit AT cycle wait state generation. Default is 5. |
| 00 | 2 wait states |
| 01 | 3 wait states |
| 10 | 4 wait states |
| 11 | 5 wait states |
| 5, 4 | 16 bit AT cycle wait state generation. Default is 3. |
| 00 | 0 wait states |
| 01 | 1 wait state |
| 10 | 2 wait states |
| 11 | 3 wait states |
| 7, 6 | Reserved.* |

*The reserved bits are recommanded to be initialized to 1.

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### 1.5 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | — | 7.0 | V |
| Input Voltage | $V_I$ | -0.5 | 5.5 | V |
| Output Voltage | $V_O$ | -0.5 | 5.5 | V |
| Operating Temperature | $T_{OP}$ | -25° | 85° | C |
| Storage Temperature | $T_{STG}$ | -40° | 125° | C |

**NOTE:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

### 1.6 82C211 Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.25 | V |
| Ambient Temperature | $T_A$ | 0° | 70° | C |

### 1.7 82C211 DC Characteristics

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | — | 0.8 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | — | V |
| Output Low Voltage $I_{OL}$ = 4mA | $V_{OL}$ | — | 0.45 | V |
| Output High Voltage $I_{OH}$ = -4mA | $V_{OH}$ | 2.4 | — | V |
| Input Current $0<V_{IN}<V_{CC}$ | $I_{IL}$ | — | ±10 | μA |
| Power Supply Current @ 16MHz | $I_{CC}$ | — | 50 | mA |
| Output High-Z Leakage Current $0.45<V_{OUT}<V_{CC}$ | $I_{OZ1}$ | | ±10 | μA |
| PROCCLK Output Low Voltage @ $I_{OL}$ = 5mA | $V_{OLC}$ | — | 0.45 | V |
| PROCCLK Output High Voltage @ $I_{OH}$ = -1mA | $V_{OHC}$ | 4.0 | — | V |
| Standby Power Supply Current | $I_{CCSB}$ | — | 1.5 | mA |

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### 1.8 82C211-12, 82C211-16 AC Characteristics

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

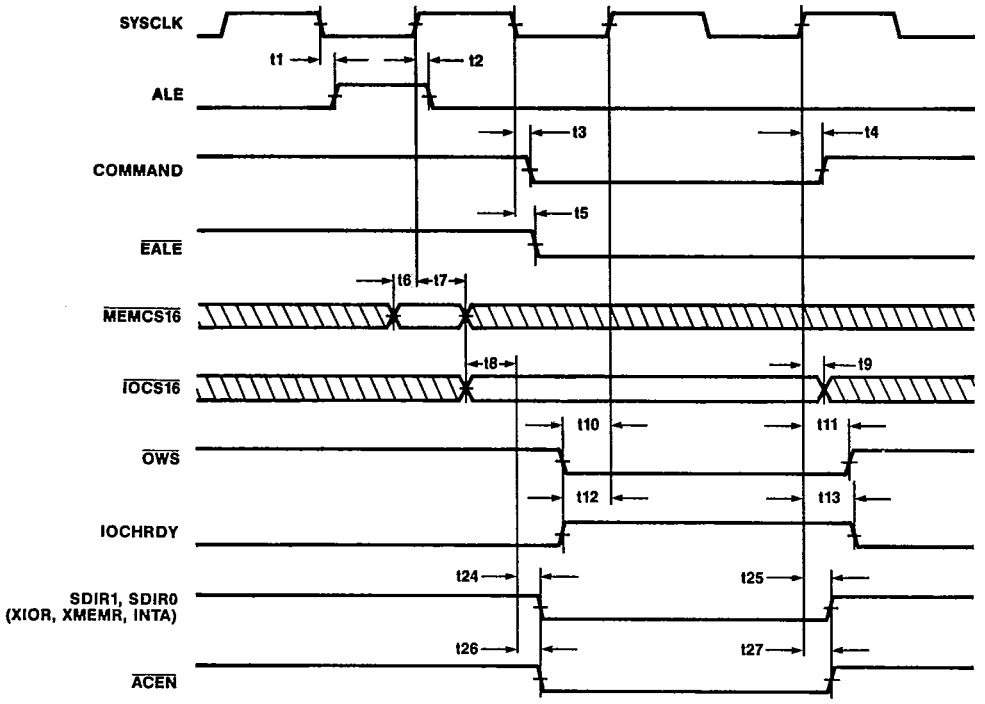
| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t1 | ALE active delay from SYSCLK↓ | –1 | | 6 (10) | ns |
| t2 | ALE inactive delay from SYSCLK↑ | –1 | | 6 (10) | ns |
| t3 | COMMAND active delay from SYSCLK↓ | 0 | | 8 | ns |
| t4 | COMMAND inactive delay from SYSCLK↑ | 0 | | 6 | ns |
| t5 | $\overline{\text{EALE}}$ active delay from SYSCLK↓ | 0 | | 10 | ns |
| t6 | $\overline{\text{MEMCS16}}$ set-up time to SYSCLK↑ | 10 | | | ns |
| t7 | $\overline{\text{MEMCS16}}$ hold time to SYSCLK↑ | 4 | | | ns |
| t8 | $\overline{\text{IOCS16}}$ set-up time to SYSCLK↓ | 10 | | | ns |
| t9 | $\overline{\text{IOCS16}}$ hold time to SYSCLK↓ | 10 | | | ns |
| t10 | $\overline{\text{0WS}}$ set-up time to SYSCLK↑ | 9 | | | ns |
| t11 | $\overline{\text{0WS}}$ hold time to SYSCLK↑ | 4 | | | ns |
| t12 | IOCHRDY set-up time to SYSCLK↑ | 11 | | | ns |
| t13 | IOCHRDY hold time to SYSCLK↑ | 4 | | | ns |
| t14 | IALE active delay from PROCCLK↓ | 1 | | 10 | ns |
| t15 | IALE inactive delay from PROCCLK↓ | 1 | | 11 (16) | ns |
| t16 | $\overline{\text{AF16}}$ set-up time to PROCCLK↓ | 15(19) | | | ns |
| t17 | $\overline{\text{AF16}}$ hold time to PROCCLK↓ | 11(13) | | | ns |
| t18 | $\overline{\text{READY}}$ input set-up time to PROCCLK↓ | 11 | | | ns |
| t19 | $\overline{\text{READY}}$ input hold time PROCCLK↓ | 8 | | | ns |
| t20 | RESET3 active delay from PROCCLK↓ | 2 | | 12 | ns |
| t21 | RESET3 inactive delay from PROCCLK↓ | 2 | | 16 | ns |
| t22 | RESET4 active delay from PROCCLK↓ | 0 | | 8 | ns |
| t23 | RESET4 inactive delay from PROCCLK↓ | 1 | | 16 | ns |
| t24 | SDIR<1:0> active delay from SYSCLK↓ | 3 | | 11 | ns |
| t25 | SDIR<1:0> inactive delay from SYSCLK↑ | 1 | | 10 | ns |
| t26 | $\overline{\text{ACEN}}$ active delay from SYSCLK↓ | 0 | | 7 | ns |
| t27 | $\overline{\text{ACEN}}$ inactive delay from SYSCLK↑ | 0 | | 6 | ns |
| t32 | AC0 active delay from PROCCLK↓ | 6 | | 17 | ns |
| t33 | AC0 inactive delay from PROCCLK↓ | 6 | | 18 | ns |
| t34 | AC1 active delay from PROCCLK↓ | 7 | | 18 | ns |

### 1.8 82C211-12, 82C211-16 AC Characteristics (Continued)
($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

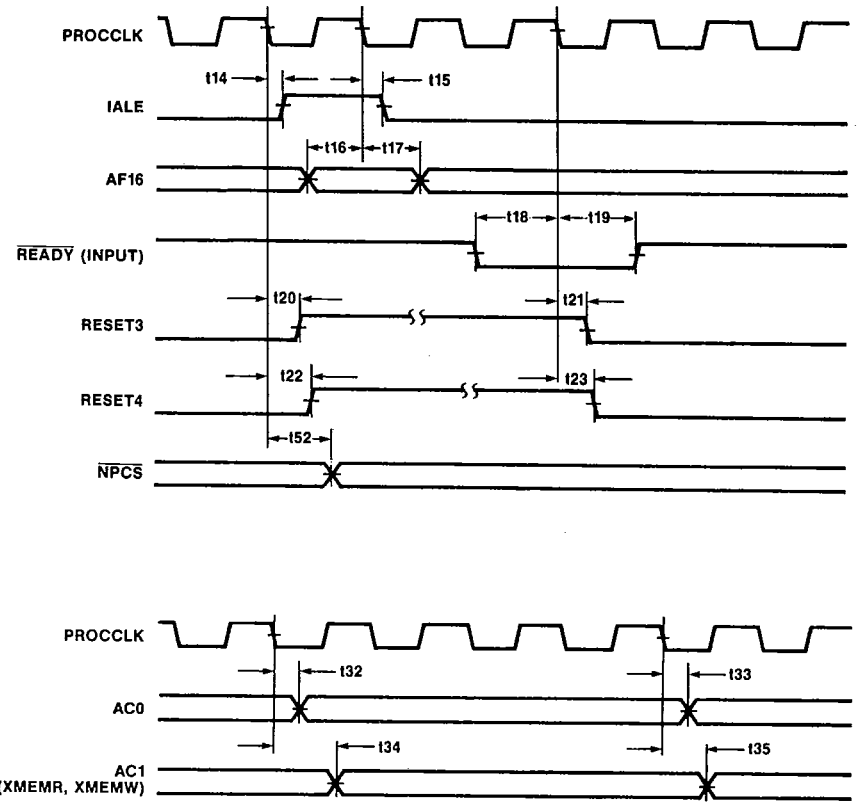
| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t35 | AC1 active delay from PROCCLK↓ | 7 | | 18 | ns |
| t38 | Hold active delay from SYSCLK↓ | 0 | | 6 | ns |
| t39 | Hold inactive delay from SYSCLK↑ | 0 | | 6 | ns |
| t40 | $\overline{REF}$ delay from HLDA | 3 | | 14 | ns |
| t43 | $\overline{REF}$ inactive delay from SYSCLK↑ | 0 | | 6 | ns |
| t44 | XMEMR active delay from SYSCLK↑ | 1 | | 9 | ns |
| t45 | XMEMR inactive delay from SYSCLK↑ | 0 | | 5 | ns |
| t46 | HRQ1 set-up to SYSCLK↑ | 10 | | | ns |
| t47 | HRQ1 hold time to SYSCLK↑ | 4 | | | ns |
| t49 | HLDA1 active delay from HLDA↑ | 8 | | 17 | ns |
| t51 | HLDA1 inactive delay from HLDA↓ | 12 | | 20 | ns |
| t52 | $\overline{NPCS}$ active delay from PROCCLK↓ | 11 | | 21 | ns |
| t53 | Overlap of $\overline{NPBUSY}$ & $\overline{ERROR}$ (both low) | 8 | | | |
| t54 | NPINT delay from $\overline{NPBUSY}$, $\overline{ERROR}$ low | 7 | | 16 | ns |
| t55 | NPINT inactive delay from $\overline{ERROR}$↑ | 3 | | 11 | ns |
| t56 | $\overline{NPBUSY}$ active pulse width | 13 | | | |
| t57 | $\overline{ERROR}$ hold time with respect to $\overline{NPBUSY}$↑ | 0 | | | |
| t58 | $\overline{ERROR}$ set up time to $\overline{NPBUSY}$↑ | 3 | | | |
| t59 | $\overline{ERROR}$ min low pulse | 8 | | | |
| t60 | $\overline{BUSY}$ active delay from $\overline{NPBUSY}$↓ | 8 | | 18 | ns |
| t61 | $\overline{BUSY}$ inactive delay from $\overline{NPBUSY}$↑ | 8 | | 15 | ns |
| t62 | $\overline{BUSY}$ delay from $\overline{IOW}$ | 2 | | 12 | ns |
| t63 | NPRST active delay from $\overline{IALE}$ | 9 | | 19 | ns |
| t64 | NPRST inactive delay from $\overline{IALE}$ | 4 | | 15 | ns |

**Note:** Values inside ( ) are 12 MHz timing.

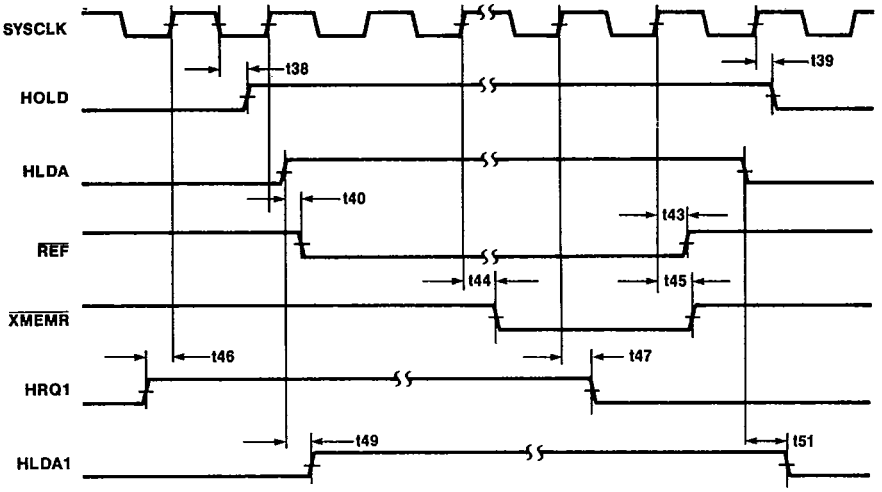
## 1.9 82C211 Timing Diagrams

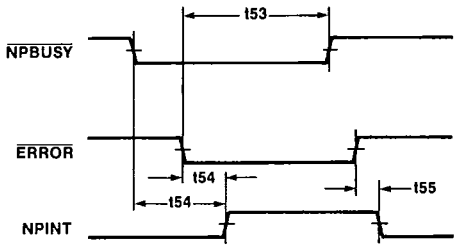


## 1.9 82C211 Timing Diagrams (Continued)

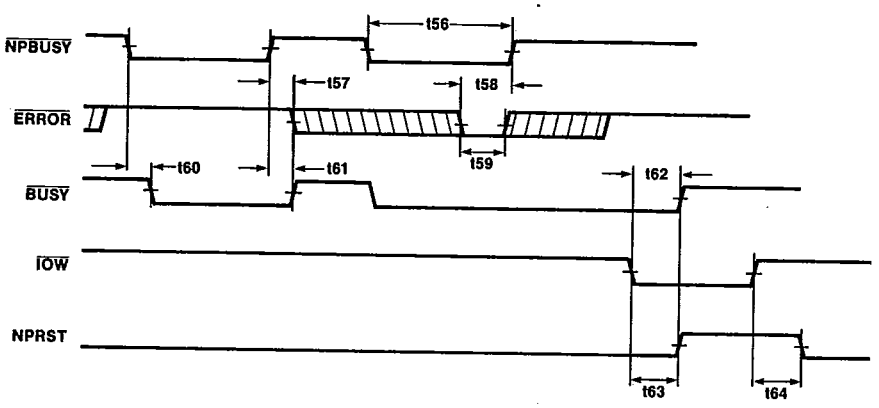


## 1.9 82C211 Timing Diagrams (Continued)



### 1.9 82C211 Timing Diagrams (Continued)



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## 2 82C212 PAGE/INTERLEAVE AND EMS MEMORY CONTROLLER

### 2.1 Features

- Page mode access including single bank, 2 way and 4 way page interleaved, providing higher performance over conventional DRAM accessing schemes
- Supports 100ns DRAMs at 16MHz using page interleaved operation
- Supports up to 8Mbytes of on board memory
- Provides automatic remapping of RAM resident in 640K to 1Mbyte area to the top of the 1Mbyte address space.
- Supports Lotus Intel Microsoft-Expanded Memory System (LIM-EMS 4.0) address translation logic
- Shadow RAM feature for efficient Basic Input/Output System (BIOS) execution
- OS/2 optimization feature allows fast switching between protected and real mode
- Staggered refresh to reduce power supply noise

### 2.2 Overview

The 82C212 performs the memory control functions in the NEAT system, utilizing page mode access DRAMs. The various memory array configurations possible and Page/Interleaved mode operation are discussed in this section. Figure 2.1 is a block diagram of the 82C212 chip.

#### 2.2.1 Array Configuration

The 82C212 organizes memory as banks of 18 bit modules, consisting of 16 bits of data

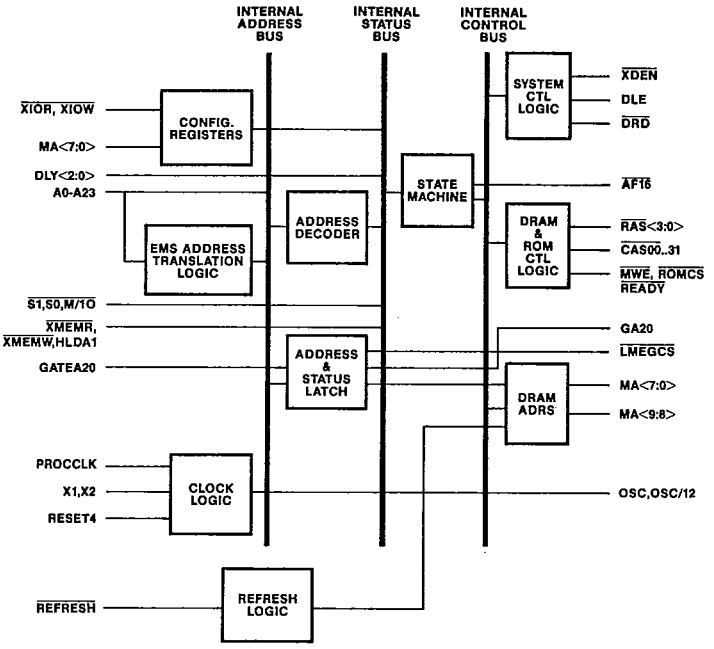


**Figure 2.1 82C212 Block Diagram**

and 2 bits of parity information. The 16 bits of data are split into high and low order bytes, with one parity bit for each byte. This configuration can be implemented by using eighteen 1-bit wide DRAMs or by using four 4-bit wide DRAMs for data with two 1-bit wide DRAMs for parity. The minimum configuration can be a single bank operating in non-interleaved mode or can be a pair of DRAM banks operating in two way interleaved mode. If the 82C212 uses a two way interleaving scheme, the DRAMs within a pair of banks must be identical. However, each bank of DRAM pairs can be different from other pairs. For example, Banks 0, 1 may have 256K by 1 bit DRAMs and Banks 2 and 3 could have 1M by 1bit DRAMs. A typical system may be shipped with one or two banks of smaller DRAM types (eg. 256K by 1 bit DRAMs) and later upgraded with additional pairs of banks of larger DRAMs (eg. 1M by 1 bit DRAMs).

### 2.2.2 Page/Interleaved Operation

The 82C212 uses a page/interleaved design that is different from most interleaved memory designs. Typical two way interleaving schemes use two banks of DRAMs with even word addresses on one bank and odd word addresses on the other bank. If memory accesses are sequential, the RAS* precharge time of one bank overlaps the access time of the other bank. Typically, programs consist of instruction fetches interspersed with operand accesses. The instruction fetches tend to be sequential and the operand accesses tend to be random.

Figure 2.2 is a sequence diagram for a memory interleaved scheme using two banks 0 and 1. The $\overline{RAS}$ signals of the two banks are interleaved so that the RAS precharge time ($T_{rp}$) of one bank is used for the $\overline{RAS}$ active time in the other bank. This requires sequential accesses to be alternating between the two banks. For non-sequential accesses, it is possible to get wait states due to a 'miss'. Typically, this results in a 50% hit ratio (possible zero wait state accesses).

Figure 2.3 is a sequence diagram of a paged mode DRAM operation. In paged mode DRAMs, once a row access has been made, it

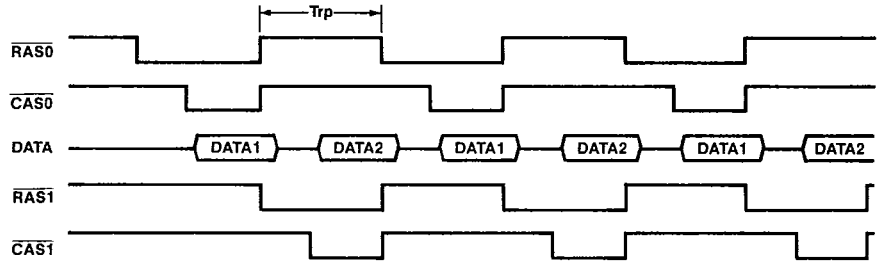


**Figure 2.2 DRAM Interleaved Operation**

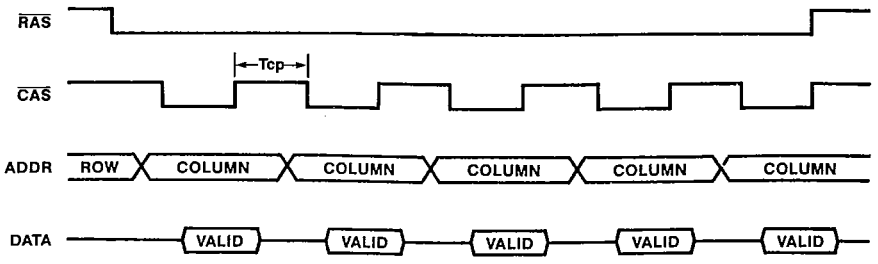


**Figure 2.3 DRAM Page Mode Operation**

is possible to access subsequent column addresses within that row, without the $\overline{RAS}$ precharge penalty. However, after a $\overline{RAS}$ active timeout, there is a $\overline{RAS}$ precharge period which typically occurs every 10 microseconds. Since the $\overline{CAS}$ precharge time $T_{cp}$ is small, it is possible to make fast random accesses within a selected row. Typically, page mode access times are half the normal DRAM access times. For 256K × 1 DRAMs, each row has 512 bits. If eighteen 256K × 1 bit DRAMs are used to implement a bank, a page would have 512 × 2 bytes (excluding 2 bits for parity) = 1 Kbytes. Thus paged mode DRAMs could be interleaved at 1 Kbyte boundaries rather than 2 byte boundaries as in the regular interleaved mode operation. Any access to the currently active $\overline{RAS}$ page would occur in a short page access time and any subsequent access could be anywhere in the same 1Kbyte boundary, without incurring any penalty due to $\overline{RAS}$ precharge. If memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving because:

1. Page mode access time is shorter than normal DRAM access time. This allows more time in the DRAM critical paths, to achieve penalty free accesses or 'hits'.
2. The possibility of the next access being fast is significantly higher than in a regular interleaving scheme. This is because instructions and data tend to cluster together by principle of locality of reference.

Figure 2.4 is a sequence diagram of a two way Page/Interleaved scheme using page mode DRAMs. As seen, it is possible to make zero wait state accesses between the two banks 0 and 1, by overlapping $\overline{CAS}$ precharge time of one bank with $\overline{CAS}$ active time of the other bank. The DRAM $\overline{RAS}$ lines for both banks can be held active till the $\overline{RAS}$ active time out period, at which time a $\overline{RAS}$ precharge for that bank is required. Typical hit ratios higher then 80% are possible using this scheme. With the 82C212 memory controller, using the page/interleaved scheme, 150 ns access time DRAMs can be used at 12MHz and 100 ns access time DRAMs at 16MHz.

82C212 supports both two and four way interleaved mode. If four way interleaved mode is used, the DRAMs used in the four banks must be identical. Table 2.0 shows the 0 wait state hit space for possible banks configurations.

**OS/2 Optimization**

The NEAT architecture features OS/2 optimization using REG6F<1> of the 82C212 in conjunction with REG60<5> of the 82C211. OS/2 makes frequent DOS calls while operating in protected mode of the 80286 CPU. In order to service these DOS calls, the 80286 CPU has to switch from protected to real mode quickly. Typical PC/AT architectures require the processor to issue two commands to the 8042 (or 8742) keyboard controller in order to reset the processor (to switch it into protected mode) and to activate GATEA20.

REG60<5> of the 82C211 is to used to invoke a software reset to the 80286 processor and REG6F<1> is used to activate GATEA20. Since this involves two I/O writes, it is possible to execute a "Fast GATEA20". In an OS/2 environment, where frequent DOS calls are made, this feature provides significant performance improvement.

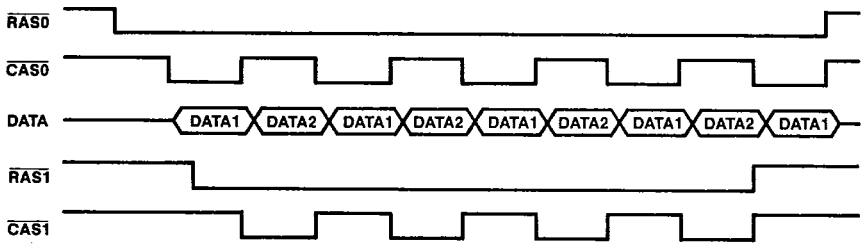


**Figure 2.4 DRAM Page/Interleave Operation**

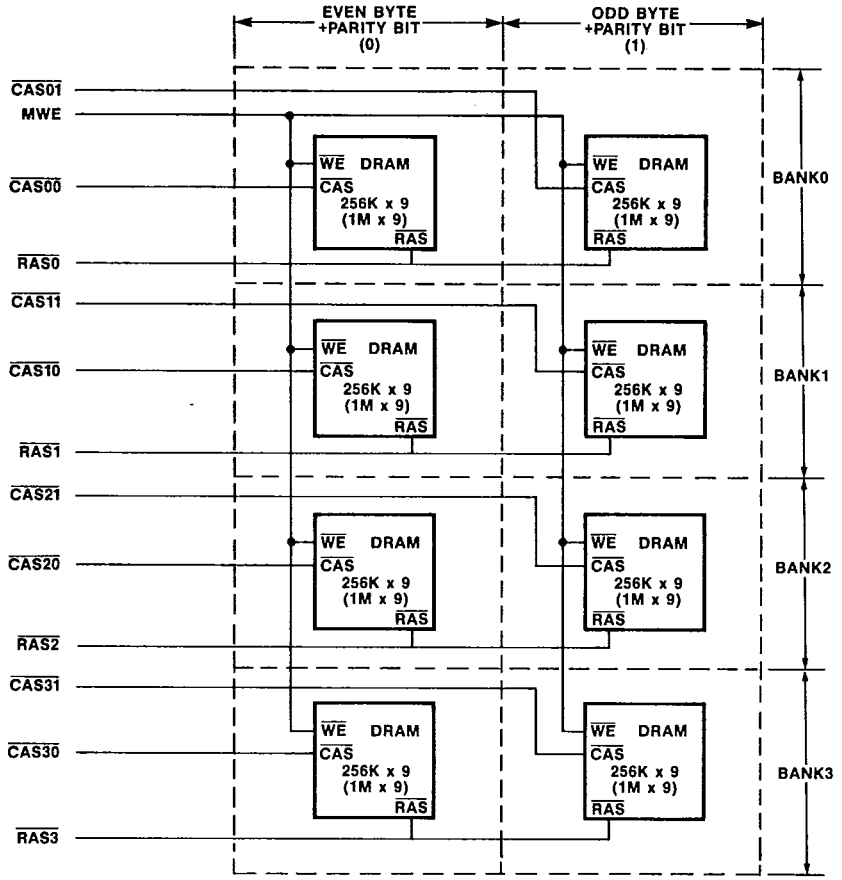


Figure 2.5 DRAM Organization

Table 2.0 Average 0 Wait State Hit Space

| DRAM Type | | | | | |
|---|---|---|---|---|---|
| Bank 0 | Bank 1 | Bank 2 | Bank 3 | Two Way Interleaved | Four Way Interleaved |
| 256K | 256K | 0 | 0 | 2K | NA |
| 256K | 256K | 256K | 256K | 2K | 4K |
| 256K | 256K | 1M | 1M | 3K | NA |
| 1M | 1M | 0 | 0 | 4K | NA |
| 1M | 1M | 1M | 1M | 4K | 8K |

## 2.3 Functional Description

Figure 2.1 is a block diagram of the 82C212 memory controller. It consists of the following sub-modules:

- EPROM and DRAM control logic
- System Control logic
- Memory Mapping and Refresh logic
- Oscillator clock generation logic
- Configuration registers

### 2.3.1 EPROM and DRAM Control Logic

The EPROM and DRAM control logic in the 82C212 is responsible for the generation of the RAS, CAS and MWE signals for DRAM accesses and the generation of ROMCS for EPROM accesses. This sub-module also generates READY to the CPU upon completion of the desired local memory operation. The appropriate number of wait states are inserted, as programmed by software (or by default) in the wait state register of the 82C212. Figure 2.5 is a block diagram of the DRAM organization for the NEAT architecture. As seen, each RAS line drives each 256K × 18 bit bank (or 1M × 18 bit bank). The CAS lines are used to drive individual bytes within each bank. MWE is connected to each DRAM bank write enable input.

### 2.3.2 System Control Logic

This sub-module of the 82C212 generates XDEN, DLE, DRD, AF16 for system control. XDEN is issued for I/O accesses to the internal registers of the 82C212. It is used to enable the XD0-7 lines onto the MA0-7 lines from an external buffer, for accessing the internal registers of the 82C212. The DLE and DRD signals are generated for enabling and controlling the direction of data between the CPU data bus and the memory data bus (MD bus). AF16 is issued by the 82C212 state machine. It is active for local memory accesses and meets the set up and hold times with respect to PROCCLK for the 82C211.

### 2.3.3 Memory Mapping and Refresh logic

The 82C212 has an extensive set of memory mapping registers for various memory organizations. The registers are discussed in section 2.3.5. Through the memory mapping logic, for up to 1 Mbyte of system RAM, it is possible to map RAM that overlaps the EPROM area (640Kbyte-1Mbyte) above the 1Mbyte area, as shown in Figure 2.6. Hence, for 1Mbyte of on board RAM, the software can address it from 0 to 640 Kbytes and from 1 Mbyte to 1.384 Mbytes. The EPROM can be addressed from the 640 Kbyte area to the 1 Mbyte area.

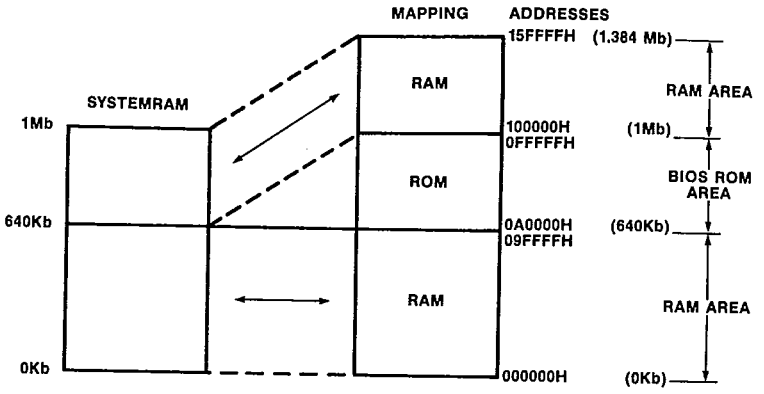


**Figure 2.6 System RAM/ROM Mapping for 1MB System RAM**

For normal mode of operation, only one bank of DRAMs may be used. However, for the page/interleaved mode of operation, RAM bank pairs must be used.

**Shadow RAM Feature**

For efficient execution of BIOS, it is preferable to execute BIOS code through RAM rather than through slower EPROMs. The 82C212 provides the shadow RAM feature which if enabled allows the BIOS code to be executed from system RAM resident at the same physical address as the BIOS EPROM. The software should transfer code stored in the BIOS EPROMs to the system RAM, before enabling the shadow RAM feature. This feature significantly improves the performance in BIOS-call intensive applications. Performance improvements as high as 300 to 400% have been observed in benckmark tests on the shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping register.

If more than 1 Mbyte of system RAM exists, it is mapped as shown in Figure 2.7, if the shadow RAM feature is not invoked. This means that RAM in the 640 Kbyte to 1 Mbyte area cannot be accessed. If the shadow RAM feature is used, then the RAM is mapped as shown in Figure 2.8, overlapping or Shadowing the EPROM area. In both cases, for accesses beyond the 1 Mbyte address range, the processor is switched from real to protected mode from BIOS.

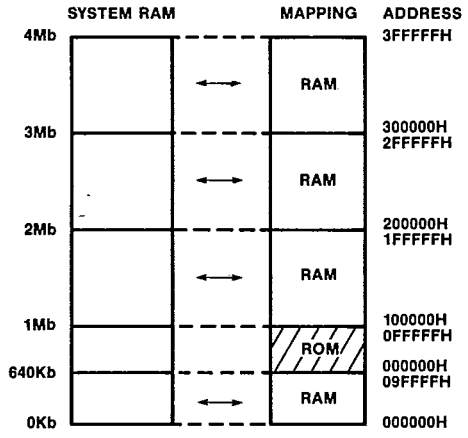


**Figure 2.7 RAM/ROM Mapping Without Shadow RAM (More Than 1MB of RAM)**

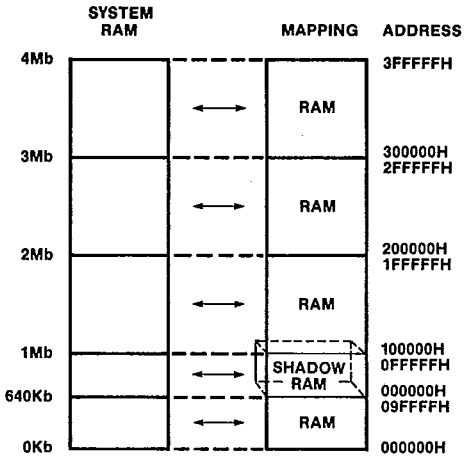


**Figure 2.8 RAM Mapping with Shadow RAM (More Than 1MB of RAM)**

**EMS Address Translation Logic**

Expanded Memory System or EMS is a memory mapping scheme used to map a 64 Kbyte block of memory in the EPROM area D0000H-DFFFFH to anywhere in the 1 Mbyte-8 Mbyte area. This 64 Kbyte memory block is segmented into four 16 Kbyte pages. Through a translation table, each 16 Kbyte segment can be mapped anywhere in the 1 Mbyte to 8 Mbyte area. Since the 82C212 uses the translation table in the EMS mode, address lines A14 to A22 are translated by the appropriate EMS mapping register. Hence, this scheme does not require switching between user and protected mode. Figure 2.9 shows the EMS organization with a possible translation scheme. It is possible for the 82C212 to map this 64 Kbyte block to anywhere in the 0 to 8 Mbyte area. However, it is desirable to map this block above the 1 Mbyte area in order to not use the RAM space in the 0 to 640 Kbyte area. Although the EMS scheme translates the 64 Kbyte block in the D0000H-DFFFFH

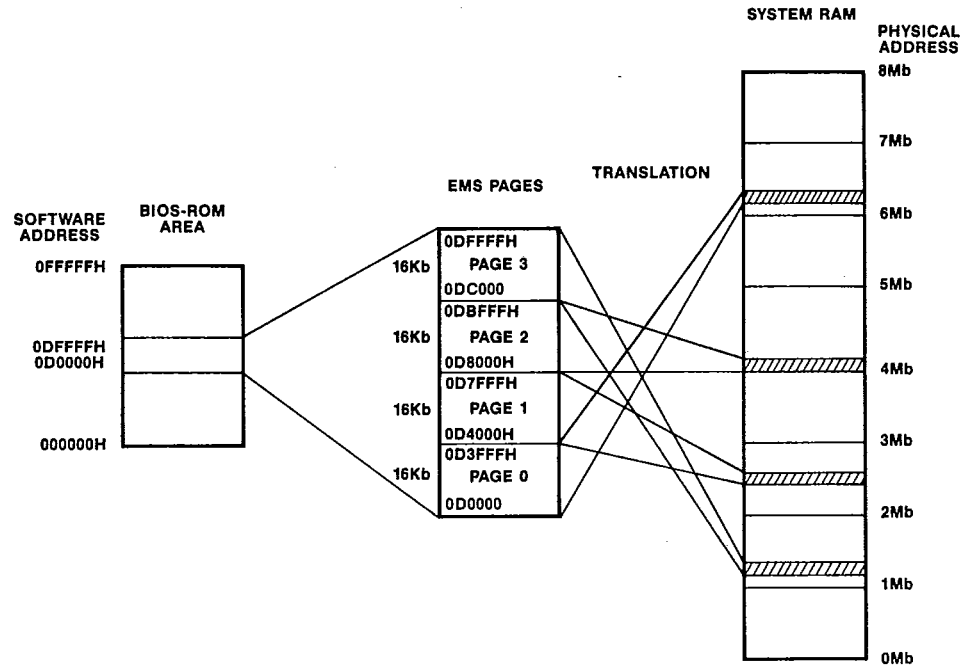


**Figure 2.9 EMS Mapping**

area, it is possible to select a 64 Kbyte block from any other area.

### Refresh Logic

During a refresh cycle, the 82C211 puts out the refresh address on the A0-A9 address lines and asserts the $\overline{REF}$ signal low to the 82C212. The 82C212 uses these signals to generate the refresh address on the MA0-MA9 address lines, the $\overline{RAS}$ signals and LMEGCS. Figure 1.5 is a sequence diagram for a refresh cycle. As seen, the 82C212 performs a staggered mode refresh to reduce the power supply noise generated during $\overline{RAS}$ switching. Prior to a refresh, all $\overline{RAS}$ lines are pulled high to ensure $\overline{RAS}$ precharge. Following this, $\overline{RAS0}$ and $\overline{RAS3}$ are asserted low. $\overline{RAS1}$ and $\overline{RAS2}$ are staggered by one delay unit using an external delay line, with respect to $\overline{RAS0}$ and $\overline{RAS3}$. The $\overline{RAS0}$-$\overline{RAS3}$, $\overline{RAS1}$-$\overline{RAS2}$ bundling is provided so that staggering is effective for a minimal 2 bank or a full 4 bank configuration.

### Memory Configurations

It is possible to use 1Mbit or 256K bit (and in one case, 64K bit) DRAMs for system memory in the NEAT CHIPSet™. Each memory bank can be implemented with eighteen 1 bit wide DRAMs or four 4 bit wide DRAMs with two 1 bit wide DRAMs. Possible configurations for onboard memory are listed in Table 2.1. Each bank is 16 bits wide plus two bits for parity.

Table 2.1

| | DRAM Type | | | | Total | EMS |
|---|---|---|---|---|---|---|
| | Bank0 | Bank1 | Bank2 | Bank3 | Memory | Range |
| 1 | 0 | 0 | 0 | 0 | disable | 0 |
| 2 | 256K | 0 | 0 | 0 | 512Kb | 0 |
| 3 | 1M | 0 | 0 | 0 | 2Mb | 1Mb to 2Mb |
| 4 | 256K | 64K | 0 | 0 | 640Kb | 0 |
| 5 | 256K | 256K | 0 | 0 | 1Mb | 1Mb to 1.384Mb |
| 6 | 1M | 1M | 0 | 0 | 4Mb | 1Mb to 4Mb |
| 7 | 256K | 256K | 256K | 0 | 1.5Mb | 1Mb to 1.5Mb |
| 8 | 256K | 256K | 1M | 0 | 3Mb | 1Mb to 3Mb |
| 9 | 1M | 1M | 1M | 0 | 6Mb | 1Mb to 6Mb |
| 10 | 256K | 64K | 256K | 256K | 1.64Mb | 1Mb to 1.64Mb |
| 11 | 256K | 256K | 256K | 256K | 2Mb | 1Mb to 2Mb |
| 12 | 256K | 64K | 1M | 1M | 4.64Mb | 1Mb to 4.64Mb |
| 13 | 256K | 256K | 1M | 1M | 5Mb | 1Mb to 5Mb |
| 14 | 1M | 1M | 1M | 1M | 8Mb | 1Mb to 8Mb |

Page/interleaving is possible for only those combinations with similar pairs of DRAMs. In table 2.1, page/interleaving is possible with combinations 5, 6, 11, 13 and 14.

### 2.4 Clock Generation Logic

The 82C212 has an oscillator circuit which uses a 14.31818 MHz crystal to generate the OSC and OSC/12 clocks. The 1.19381 MHz OSC/12 clock is used internally to generate the $\overline{RAS}$ timeout clocks, one for each bank. $\overline{RAS}$ is deasserted for each bank when its $\overline{RAS}$ time out counter times out after about 10 microseconds.

### 2.5 Configuration Registers

There are twelve configuration and diagnostics registers in the 82C212, RB0-RB11. These are accessed through IO ports 22H and 23H normally found in the interrupt controller module of the 82C206 IPC. An indexing scheme is used to reduce the number of I/O addresses required to access all of the registers needed to configure and control the memory controller. Port 22H is used as an index register that points to the required data value accessed through port 23H. A write of the index value for the required data is performed to location 22H. This is then decoded and controls the multiplexers gating the appropriate register to the output bus. Every access to port 23H must be preceded by a write of the index value to port 22H even if the same data register is being accessed again. All bits marked as Reserved are set to zero by default and must be maintained that way during write operations. Table 2.2 lists these registers.

**Table 2.2**

| Register Number | Register Name | Index |
|---|---|---|
| RB0 | Version | 64H |
| RB1 | ROM Configuration | 65H |
| RB2 | Memory Enable-1 | 66H |
| RB3 | Memory Enable-2 | 67H |
| RB4 | Memory Enable-3 | 68H |
| RB5 | Memory Enable-4 | 69H |
| RB6 | Bank 0/1 Enable | 6AH |
| RB7 | DRAM Configuration | 6BH |
| RB8 | Bank 2/3 Enable | 6CH |
| RB9 | EMS Base Address | 6DH |
| RB10 | EMS Address Extension | 6EH |
| RB11 | Miscellaneous | 6FH |

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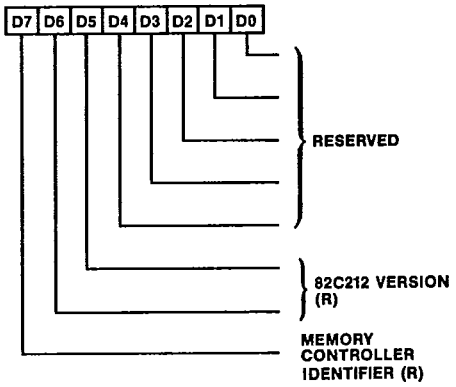
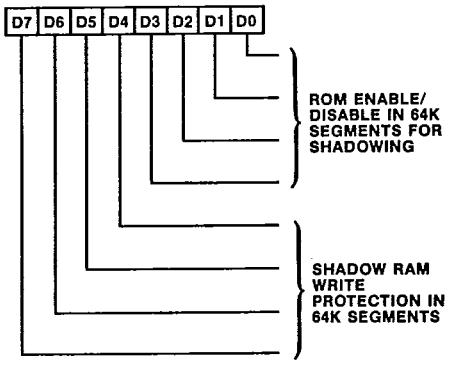
### 2.5.1 Register Description

**Version Register RB0**
Index register port: 22H
Data register port: 23H
Index: 64H



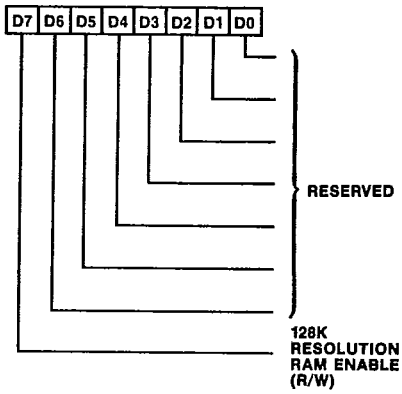

| Bits | Function |
|---|---|
| 7 | NEAT memory controller identifier. 0 = 82C212 |
| 6, 5 | 82C212 revision number. 00 = initial revision number |
| 4-0 | Reserved and default to 0* |

**ROM Configuration Register RB1**
Index register port: 22H
Data register port: 23H (R/W)
Index: 65H



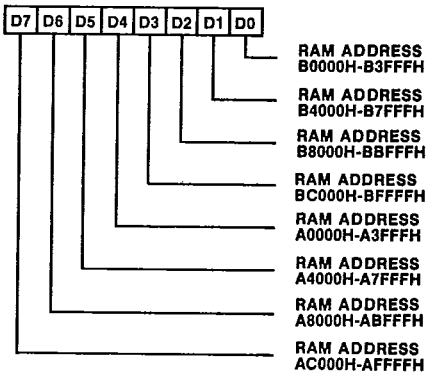

| Bits | Function |
|---|---|
| 0 | ROM at F0000H-FFFFFH (BIOS). Default = 0 = ROM enabled. ROMCS is generated. |
| 1 | ROM at E0000H-EFFFFH. Default = 1 = ROM disabled, Shadow RAM enabled. ROMCS is not generated unless bit is set to 0. |
| 2 | ROM at D0000H-DFFFFH. Default = 1 = ROM disabled, Shadow RAM enabled. ROMCS is not generated unless bit is set to 0. |
| 3 | ROM at C0000H-CFFFFH (EGA). Default = 1 = ROM disabled, Shadow RAM enabled. ROMCS is not generated unless bit is set to 0. |
| 4 | Shadow RAM at F0000H-FFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected). |
| 5 | Shadow RAM at E0000H-EFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected). |
| 6 | Shadow RAM at D0000H-DFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected). |
| 7 | Shadow RAM at C0000H-CFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected). |

**Memory Enable-1 Register RB2**
Index register port: 22H
Data register port: 23H
Index: 66H



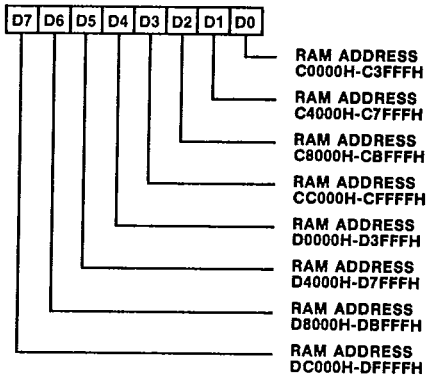

| Bits | Function |
|---|---|
| 0-6 | Reserved and default to 0* |
| 7 | Address map RAM on system board in 80000H-9FFFFH area. 0 = Address is on the I/O channel (Default), 1 = Address is on the system board and is put out by the 82C212. |

**Memory Enable Register-2 RB3**
Index register port: 22H
Data register port: 23H (R/W)
Index: 67H




| Bits | Function |
|---|---|
| 0 | Enable Shadow RAM in B0000H-B3FFFH area. Disable = 0 Enable = 1. |
| 1 | Enable Shadow RAM in B4000H-B7FFFH rea. Disable = 0 Enable = 1. |
| 2 | Enable Shadow RAM in B8000H-BBFFFH area. Disable = 0 Enable = 1. |
| 3 | Enable Shadow RAM in BC000H-BFFFFH area. Disable = 0 Enable = 1. |
| 4 | Enable Shadow RAM in A0000H-A3FFFH area. Disable = 0 Enable = 1. |
| 5 | Enable Shadow RAM in A4000H-A7FFFH area. Disable = 0 Enable = 1. |
| 6 | Enable Shadow RAM in A8000H-ABFFFH area. Disable = 0 Enable = 1. |
| 7 | Enable Shadow RAM in AC000H-AFFFFH area. Disable = 0 Enable = 1. |

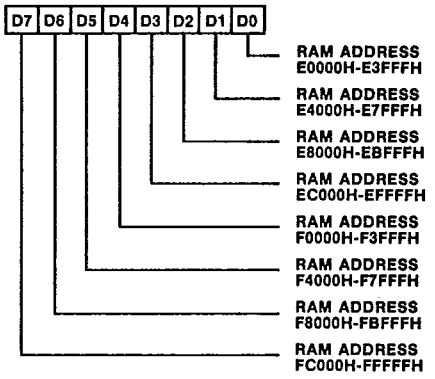
**Memory Enable-3 Register RB4**
Index register port: 22H
Data register port: 23H (R/W)
Index: 68H




| Bits | Function |
|---|---|
| 0 | Enable Shadow RAM in C0000H-C3FFFH area. Disable = 0 Enable = 1. |
| 1 | Enable Shadow RAM in C4000H-C7FFFH area. Disable = 0 Enable = 1. |

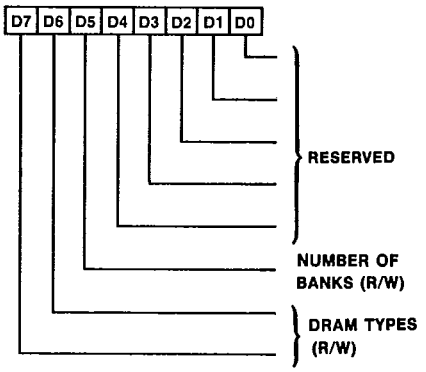
| | |
|---|---|
| 2 | Enable Shadow RAM in C8000H-CBFFFH area. Disable = 0 Enable = 1. |
| 3 | Enable Shadow RAM in CC000H-CFFFFH area. Disable = 0 Enable = 1. |
| 4 | Enable Shadow RAM in D0000H-D3FFFH area. Disable = 0 Enable = 1. |
| 5 | Enable Shadow RAM in D4000H-D7FFFH area. Disable = 0 Enable = 1. |
| 6 | Enable Shadow RAM in D8000H-DBFFFH area. Disable = 0 Enable = 1. |
| 7 | Enable Shadow RAM in DC000H-DFFFFH area. Disable = 0 Enable = 1. |

**Memory Enable-4 Register (RB5)**
Index register port: 22H
Data register port: 23H (R/W)
Index: 69H




| Bits | Function |
|---|---|
| 0 | Enable Shadow RAM in E0000H-E3FFFH area. Disable = 0 Enable = 1. |
| 1 | Enable Shadow RAM in E4000H-E7FFFH area. Disable = 0 Enable = 1. |
| 2 | Enable Shadow RAM in E8000H-EBFFFH area. Disable = 0 Enable = 1. |
| 3 | Enable Shadow RAM in EC000H-EFFFFH area. Disable = 0 Enable = 1. |
| 4 | Enable Shadow RAM in F0000H-F3FFFH area. Disable = 0 Enable = 1. |
| 5 | Enable Shadow RAM in F4000H-F7FFFH area. Disable = 0 Enable = 1. |
| 6 | Enable Shadow RAM in F8000H-FBFFFH area. Disable = 0 Enable = 1. |
| 7 | Enable Shadow RAM in FC000H-FFFFFH area. Disable = 0 Enable = 1. |

**Bank 0/1 Enable Register RB6**
Index register port: 22H
Data register port: 23H
Index: 6AH




| Bits | Function |
|---|---|
| 0-4 | Reserved and default to 0* |
| 5 | Number of RAM banks used. 0 = one bank, non-interleaved mode (Default), 1 = two banks |
| 7, 6 | These bits contain the information for the DRAM types used on the system board. POST/BIOS should use the DRAM configuration data stored in the CMOS RAM of the 82C206 IPC. |

| 7 | 6 | DRAM Types |
|---|---|---|
| 0 | 0 | Disabled |
| 0 | 1 | 256K and 64K bit DRAMs used (for 640 Kbyte combination only) |
| 1 | 0 | 256K bit DRAMs used (Default) |
| 1 | 1 | 1M bit DRAMs used |

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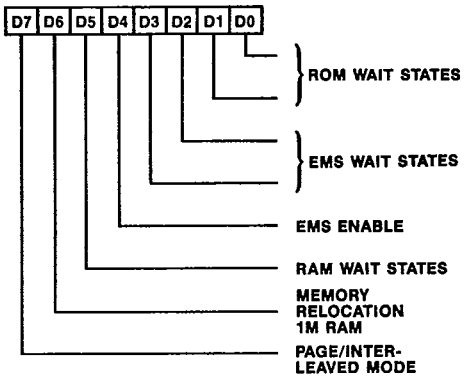
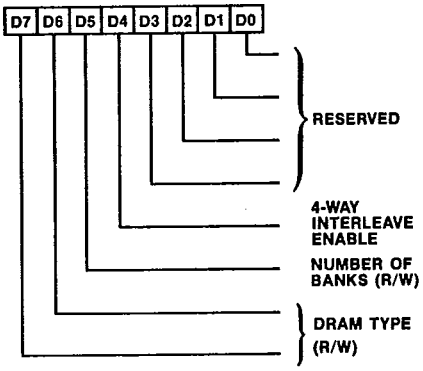
**DRAM Configuration Register RB7**
Index register port: 22H
Data register port: 23H (R/W)
Index: 6BH




| Bits | Function |
|---|---|
| 1, 0 | ROM access wait states control.<br>1 0 Wait States<br>0 0 0<br>0 1 1<br>1 0 2<br>1 1 3 (Default) |
| 3, 2 | EMS memory access wait states.<br>3 2 Wait States<br>0 0 0 |
| 4 | EMS enable bit.If set to 0, EMS is disabled (Default). If set to 1, EMS is enabled. |
| 5 | RAM access wait states. If set to 0, accesses have 0 wait state. If set to 1 (Default), accesses will have 1 wait state. |
| 6 | 640Kbyte to 1Mbyte RAM relocation bit. A zero does not relocate local RAM. A one (Default) relocates local RAM from 0A0000-0FFFFF to 100000H-15FFFFH, provided total local RAM is 1 Mbyte only. |
| 7 | Page/Interleaved mode enable. A 0 disables the page/interleaved mode, allowing useage of normal mode for the DRAMs (Default). A 1 enables page/interleaved mode for the DRAMs. |

**Bank 2/3 Enable Register RB8**
Index register port: 22H
Data register port: 23H
Index: 6CH




| Bits | Function |
|---|---|
| 0-3 | Reserved and default to 0* |
| 4 | A zero enable the 2-way page interleaved mode. A one (Default) enables the 4-way page interleaved mode if all 4 banks are the same DRAM devices. |
| 5 | Number of local RAM banks used. 0 = one bank used, non-interleaved mode only (Default). 1 = two banks used. |
| 7, 6 | These bits indicate the local DRAM type as listed:<br>7 6 DRAM Type<br>0 0 none (Default)<br>0 1 Reserved<br>1 0 256 Kbit<br>1 1 1 Mbit |

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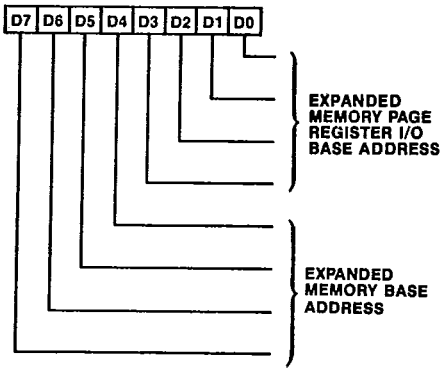
**EMS Base Address Register RB9**
Index register port: 22H
Data register port: 23H (R/W)
Index: 6DH



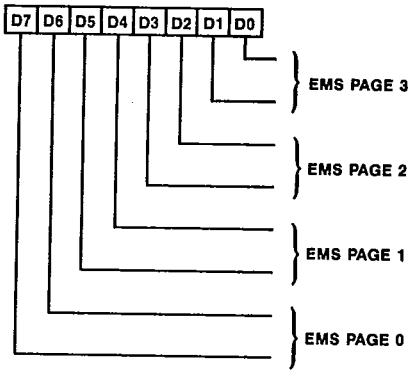

| Bits | Function |
|---|---|
| 0-3 | These bits are used for the EMS page register I/O base address. The bits are encoded as follows, with unused combinations being reserved: |

| 3 | 2 | 1 | 0 | I/O Base |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 208H/209H |
| 0 | 0 | 0 | 1 | 218H/219H |
| 0 | 1 | 0 | 1 | 258H/259H |
| 0 | 1 | 1 | 0 | 268H/269H |
| 1 | 0 | 1 | 0 | 2A8H/2A9H |
| 1 | 0 | 1 | 1 | 2B8H/2B9H |
| 1 | 1 | 1 | 0 | 2E8H/2E9H |

7-4 These bits are used for selecting the expanded memory base addresses. They are encoded as follows, with all unused combinations being reserved:

| 7 | 6 | 5 | 4 | EMS Base Addresses |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | C0000H, C4000H, C8000H, CC000H |
| 0 | 0 | 0 | 1 | C4000H, C8000H, CC000H, D0000H |
| 0 | 0 | 1 | 0 | C8000H, CC000H, D0000H, D4000H |
| 0 | 0 | 1 | 1 | CC000H, D0000H, D4000H, D8000H |
| 0 | 1 | 0 | 0 | D0000H, D4000H, D8000H, DC000H |
| 0 | 1 | 0 | 1 | D4000H, D8000H, DC000H, E0000H |
| 0 | 1 | 1 | 0 | D8000H, DC000H, E0000H, E4000H |
| 0 | 1 | 1 | 1 | DC000H, E0000H, E4000H, E8000H |
| 1 | 0 | 0 | 0 | E0000H, E4000H, E8000H, EC000H |

**EMS Address Extention Register RB10**
Index register port: 22H
Data register port: 23H (R/W)
Index: 6EH




| Bits | Function |
|---|---|
| 1(A22) 0(A21) | EMS Page 3 address extension bits. |

| 1 | 0 | Block of EMS Memory |
|---|---|---|
| 0 | 0 | 0 Mbyte to 2 Mbyte |
| 0 | 1 | 2 Mbyte to 4 Mbyte |
| 1 | 0 | 4 Mbyte to 6 Mbyte |
| 1 | 1 | 6 Mbyte to 8 Mbyte |

| Bits | Function |
|---|---|
| 3(A22) 2(A21) | EMS Page 2 address extension bits. |

| 3 | 2 | Block of EMS Memory |
|---|---|---|
| 0 | 0 | 0 Mbyte to 2 Mbyte |
| 0 | 1 | 2 Mbyte to 4 Mbyte |
| 1 | 0 | 4 Mbyte to 6 Mbyte |
| 1 | 1 | 6 Mbyte to 8 Mbyte |

| | |
|---|---|
| 5(A22)<br>4(A21) | EMS Page 1 address extension bits. |

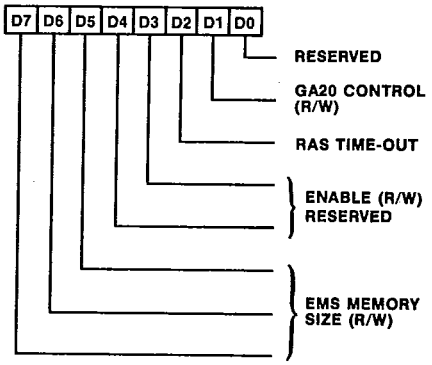
| 5 | 4 | Block of EMS Memory |
|---|---|---|
| 0 | 0 | 0 Mbyte to 2 Mbyte |
| 0 | 1 | 2 Mbyte to 4 Mbyte |
| 1 | 0 | 4 Mbyte to 6 Mbyte |
| 1 | 1 | 6 Mbyte to 8 Mbyte |

| | |
|---|---|
| 7(A22)<br>6(A21) | EMS Page 0 address extension bits. |

| 7 | 6 | Block of EMS Memory |
|---|---|---|
| 0 | 0 | 0 Mbyte to 2 Mbyte |
| 0 | 1 | 2 Mbyte to 4 Mbyte |
| 1 | 0 | 4 Mbyte to 6 Mbyte |
| 1 | 1 | 6 Mbyte to 8 Mbyte |

Address lines A22 and A21 are used in EMS Address translation logic.

**Miscellaneous Register RB12**
Index register port: 22H
Data register port: 23H
Index: 6FH




| Bits | Function |
|---|---|
| 0 | Reserved and default to 0.* |
| 1 | This bit is used for Address line A20 control and provides OS/2 optimization while switching between real and protected modes: If the bit is set to 0 it enables CPUA20 onto A20. The bit default to 1 and sets A20 = 0. |
| 2 | This bit is used to enable the RAS time-out counter for page mode operation. The counter is disabled if set to 0 (Default) and is enabled if set to 1. |
| 3, 4 | Reserved and default to 1 (bit 4), 0 (bit 3). |
| 7-5 | These bits are used to set the EMS memory space according to the following coding: |

| 7 | 6 | 5 | EMS Memory Size |
|---|---|---|---|
| 0 | 0 | 0 | less than 1 Mbyte |
| 0 | 0 | 1 | 1 Mbyte |
| 0 | 1 | 0 | 2 Mbytes |
| 0 | 1 | 1 | 3 Mbytes |
| 1 | 0 | 0 | 4 Mbytes |
| 1 | 0 | 1 | 5 Mbytes |
| 1 | 1 | 0 | 6 Mbytes |
| 1 | 1 | 1 | 7 Mbytes |

**EMS Page Registers**

| | |
|---|---|
| Page 0 | 2X8/2X9H |
| Page 1 | 42X8/42X9H |
| Page 2 | 82X8/82X9H |
| Page 3 | C2X8/C2X9H |

| Bits | Function |
|---|---|
| 0-6 | 0 - A14<br>1 - A15<br>2 - A16<br>3 - A17<br>4 - A18<br>5 - A19<br>6 - A20 |
| 7 | 0 - page disable<br>1 - page enable |

X can be 0, 1, 5, 6, A, B, E

*The reserved bits are recommanded to be initialized to 1.

### 2.6 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | — | 7.0 | V |
| Input Voltage | $V_I$ | -0.5 | 5.5 | V |
| Output Voltage | $V_O$ | -0.5 | 5.5 | V |
| Operating Temperature | $T_{OP}$ | -25° | 85° | C |
| Storage Temperature | $T_{STG}$ | -40° | 125° | C |

**NOTE:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

### 2.7 82C212 Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.25 | V |
| Ambient Temperature | $T_A$ | 0° | 70° | C |

### 2.8 82C212 DC Characteristics

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | — | 0.8 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | — | V |
| Output Low Voltage $I_{OL}$ = 4mA | $V_{OL}$ | — | 0.45 | V |
| Output High Voltage $I_{OH}$ = -4mA | $V_{OH}$ | 2.4 | — | V |
| Input Low Current $0<V_{IN}<V_{CC}$ | $I_{IL}$ | — | +10 | μA |
| Power Supply Current @ 16MHz | $I_{CC}$ | — | 75 | mA |
| Output High-Z Leakage Current $0.45<V_{OUT}<V_{CC}$ | $I_{OZ1}$ | | +10 | μA |
| Standby Power Supply Current | $I_{CCSB}$ | — | 1.0 | mA |

## 2.9 82C212-12, 82C212-16 AC Characteristics

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t1 | $\overline{RAS_i}$ active delay from CLK2↓ | 11 | | 16 | ns |
| t2 | $\overline{RAS_i}$ inactive delay from CLK2↓ | 15 | | 25 | ns |
| t3 | DLYOUT active delay from $\overline{RAS_i}$↓ | 0 | | 4 | ns |
| t4 | DLYOUT inactive delay from $\overline{RAS_i}$↑ | 0 | | 6 | ns |
| t5 | Column address stable from DLY0↑ | 8 | | 18 | ns |
| t6 | Column address hold from DLY0↓ | 6 | | | ns |
| t7 | $\overline{CAS_i}$ active delay from DLY1↑ | 7 | | 14 | ns |
| t8 | $\overline{CAS_i}$ inactive delay from DLY1↓ | 11 | | 18 | ns |
| t9 | $\overline{AF16}$ active delay from CLK2↓ | 7 | | 16(19) | ns |
| t10 | $\overline{AF16}$ inactive delay from CLK2↓ | 8 | | 18(21) | ns |
| t11 | $\overline{READY}$ active delay from CLK2↓ | 15 | | 25 | ns |
| t12 | $\overline{READY}$ inactive delay from CLK2↓ | 11 | | 20 | ns |
| t13 | $\overline{DRD}$ active delay from CLK2↓ | 10 | | 19 | ns |
| t14 | $\overline{DRD}$ hold from DLE↓ | 13 | | | ns |
| t15 | DLE active delay from $\overline{DLY1}$↑ | 6 | | 16 | ns |
| t16 | DLE inactive delay from CLK2↓ | 9 | | 18 | ns |
| t17 | $\overline{LMEGCS}$ active from CLK2↓ | 12 | | 21 | ns |
| t18 | $\overline{LMEGCS}$ inactive from CLK2↓ | 11 | | 20 | ns |
| t19 | $\overline{GA20}$ valid delay from CPU <A20> valid | 7 | | 16 (20) | ns |
| t20 | $\overline{GA20}$ invalid delay from CPU <A20> invalid | 4 | | 12 (16) | ns |
| t22 | $\overline{MWE}$ active delay from CLK2↓ | 11 | | 20 | ns |
| t23 | $\overline{MWE}$ inactive delay from CLK2↑ | 4 | | 12 | ns |
| t26 | $\overline{CAS_i}$ active delay from CLK2↓ | 10 | | 19 (25) | ns |
| t27 | $\overline{CAS_i}$ inactive delay from CLK2↓ | 11 | | 21(26) | ns |
| t28 | $\overline{DRD}$ inactive delay from CLK2↓ | 12 | | 23 | ns |
| t29 | $\overline{CAS_i}$ inactive delay from DLE inactive | 2 | | | ns |
| t30 | $\overline{RAS_i}$ active delay from CLK2↓ | 10.5 | | 16 | ns |
| t31 | Row address set up time to $\overline{RAS_i}$↓ | 8 | | | ns |
| t32 | Row address hold time from CLK2↓ | 6 | | 22 | ns |
| t33 | $\overline{RAS_i}$ inactive delay from CLK2↓ | 15 | | 25 | ns |

## 2.9 82C212-12, 82C212-16 AC Characteristics (Continued)

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t34 | $\overline{RAS_i}$ precharge time (Interleaved Mode) | | 4 × CLK2 | | |
| t35 | $\overline{ROMCS}$ active from CLK2↓ | | 11 | 20 | ns |
| t36 | $\overline{ROMCS}$ inactive from CLK2↓ | | 10 | 20 | ns |
| t37 | DLE hold time from $\overline{DRD}$ | | 0 | 7 | ns |
| t38 | $\overline{RAS_{0-3}}$ inactive from $\overline{REF}$↓ | | 13 | 24 | ns |
| t39 | $\overline{RAS_{0,3}}$ active from $\overline{XMEMR}$↓ | | 9 | 17 | ns |
| t40 | $\overline{RAS_{0,3}}$ inactive from $\overline{XMEMR}$↑ | | 10 | 19 | ns |
| t41 | $\overline{RAS_{1,2}}$ active from $\overline{RAS_{0,3}}$↓ | | 7 | 15 | ns |
| t42 | $\overline{RAS_{1,2}}$ inactive from $\overline{RAS_{0,3}}$↑ | | 11 | 20 | ns |
| t43 | Address setup time from $\overline{XMEMR}$↓ | | 10 | | ns |
| t44 | Address hold time from $\overline{REF}$↑ | | 4 | | ns |
| t45 | Refresh address delay | | 0 | | ns |
| t47 | $\overline{LMEGCS}$ delay from $\overline{REF}$↓ | | 8 | 16 | ns |
| t48 | $\overline{LMEGCS}$ delay from $\overline{REF}$↑ | | 10 | 19 | ns |
| t49 | $\overline{RAS_{0-3}}$ inactive from HLDA1↑ | | 11 | 20 | ns |
| t50 | $\overline{RAS_i}$ active from command active | | 10 | 18 | ns |
| t51 | $\overline{RAS_i}$ inactive from command inactive | | 12 | 21 | ns |
| t54 | Column address stable from DLY0↑ | | 9 | 18 | ns |
| t55 | $\overline{CAS_i}$ active delay from DLY1↑ (while XMEMW active) | | 6 | 14 | ns |
| t56 | $\overline{CAS_i}$ inactive delay from command inactive | | 9 | 18 | ns |
| t57 | $\overline{AF16}$ active from command active | | 9 | 17 | ns |
| t58 | $\overline{AF16}$ inactive from command inactive | | 6 | 14 | ns |

**Note:** Value inside ( ) are 12 MHz timing.

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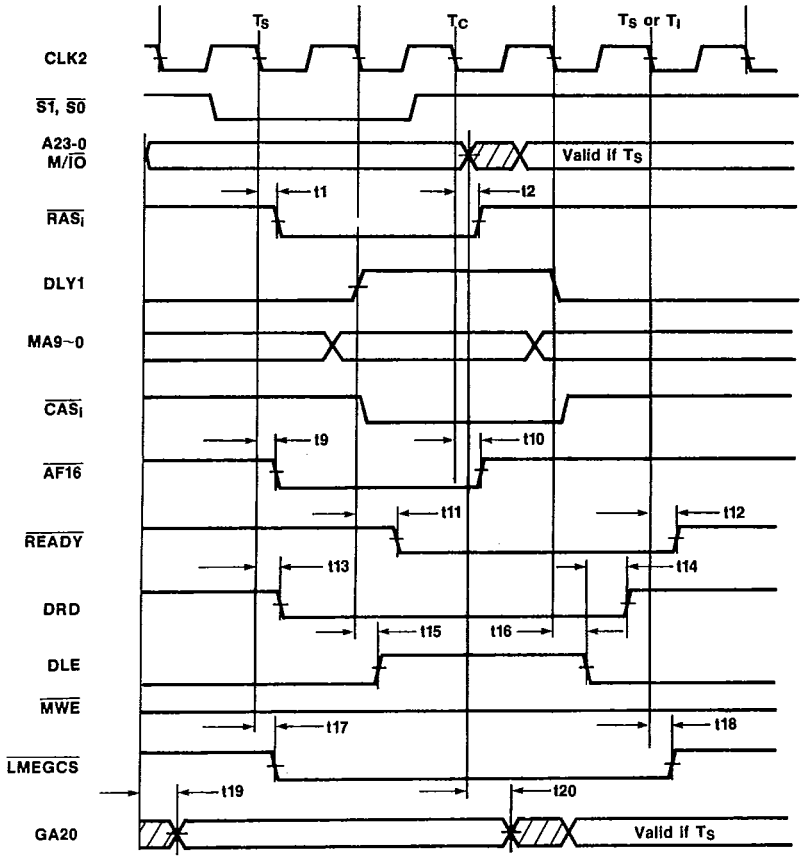
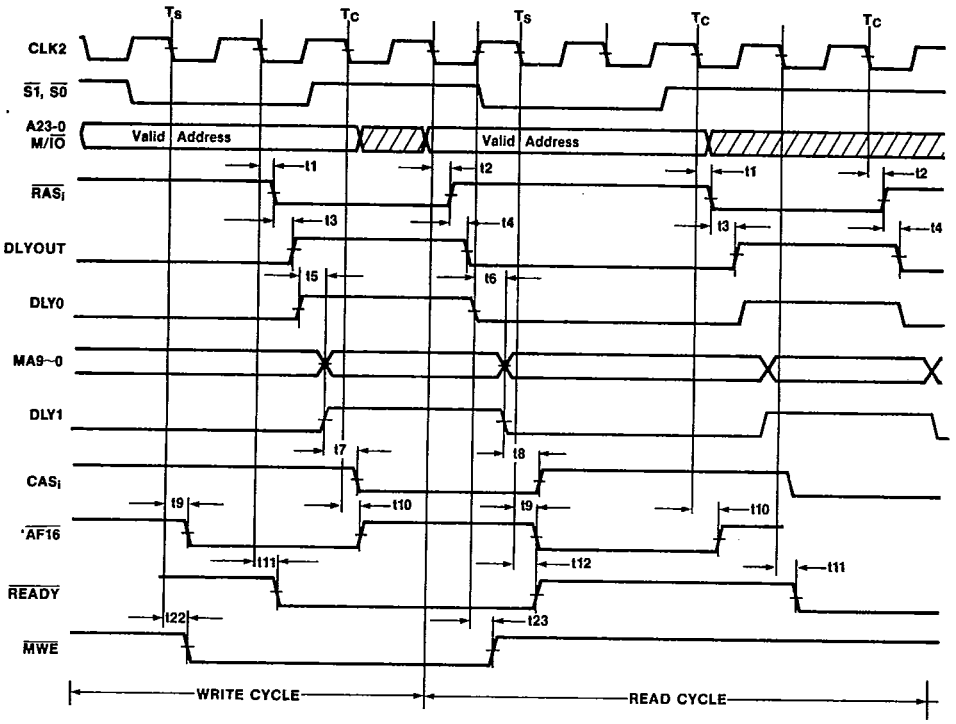
## 2.10 82C212 Timing Diagrams



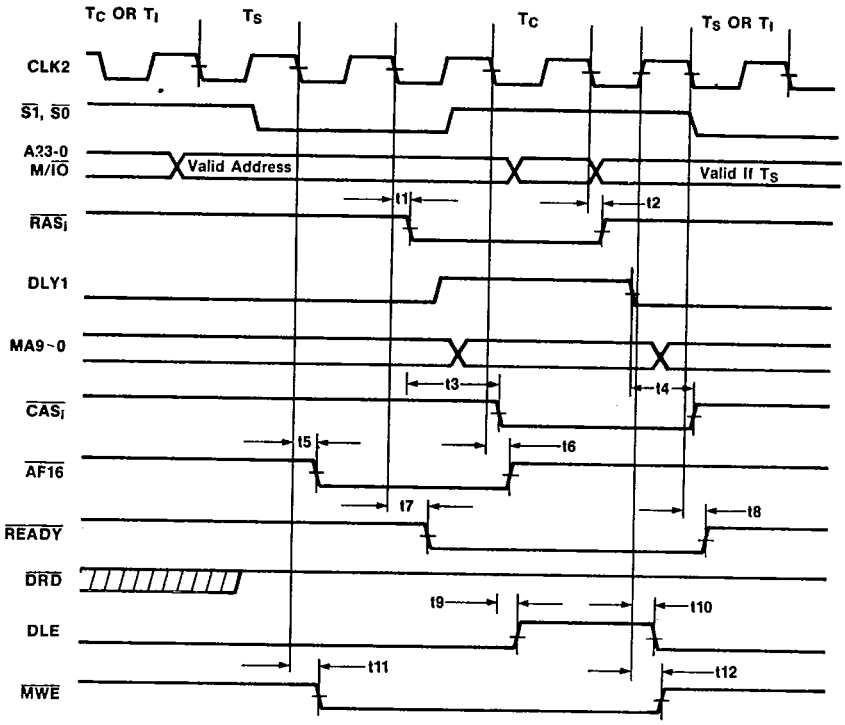

**Non-Interleave Mode—Read, 0WS**

## 2.10 82C212 Timing Diagrams (Continued)



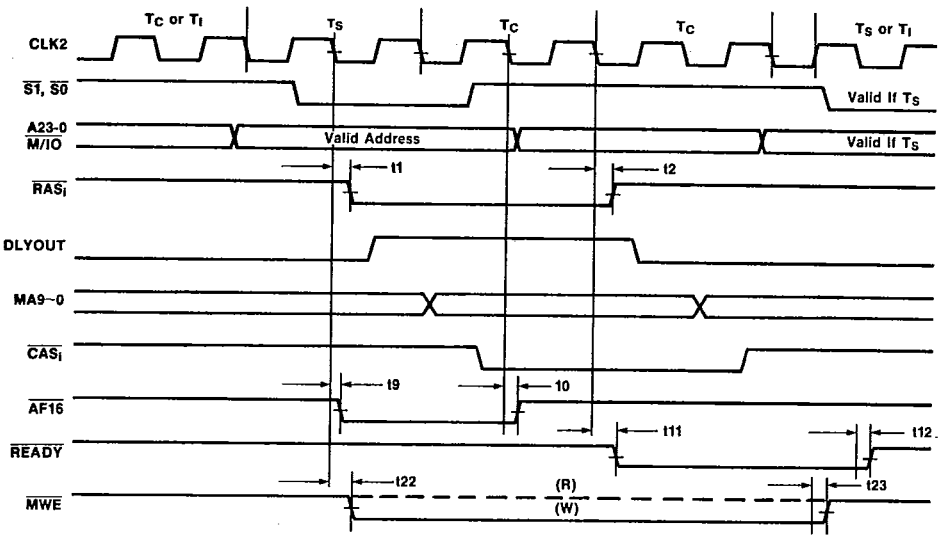

**Non-Interleave Mode—Write Followed by Read, 0WS**

## 2.10 82C212 Timing Diagrams (Continued)



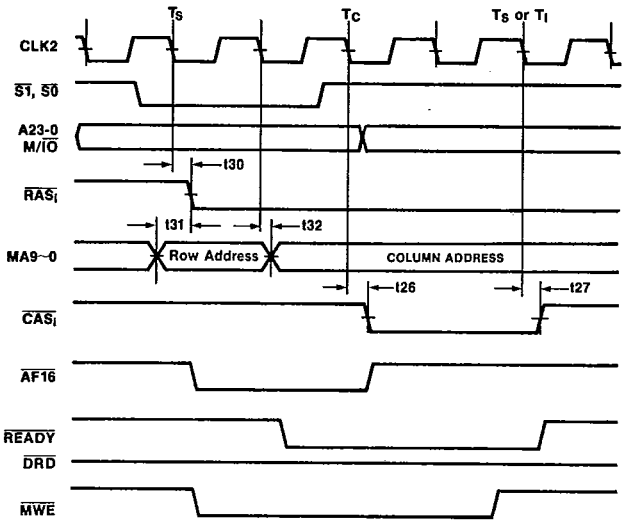

**Non-Interleave Mode—0WS, Write**

## 2.10 82C212 Timing Diagrams (Continued)



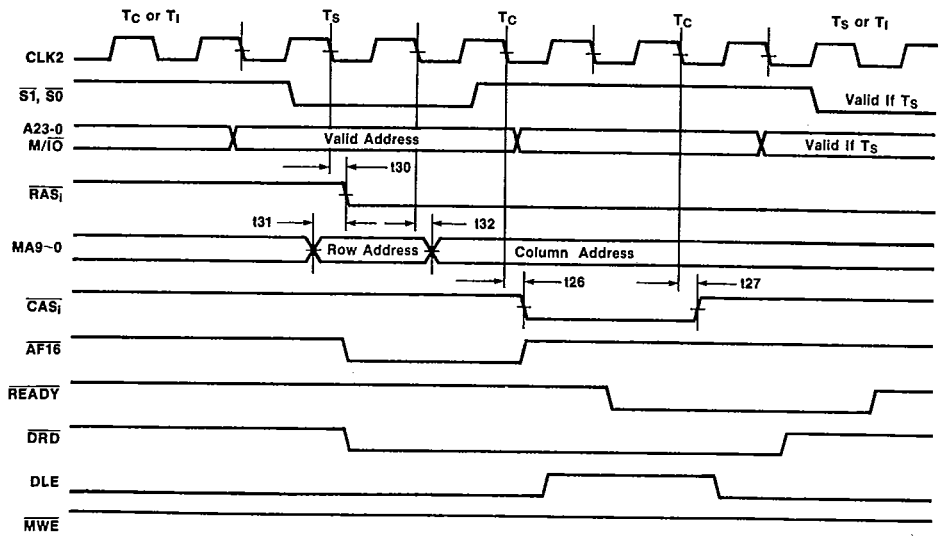

**Non-Interleave Mode—1WS, Read, Write**

## 2.10 82C212 Timing Diagrams (Continued)



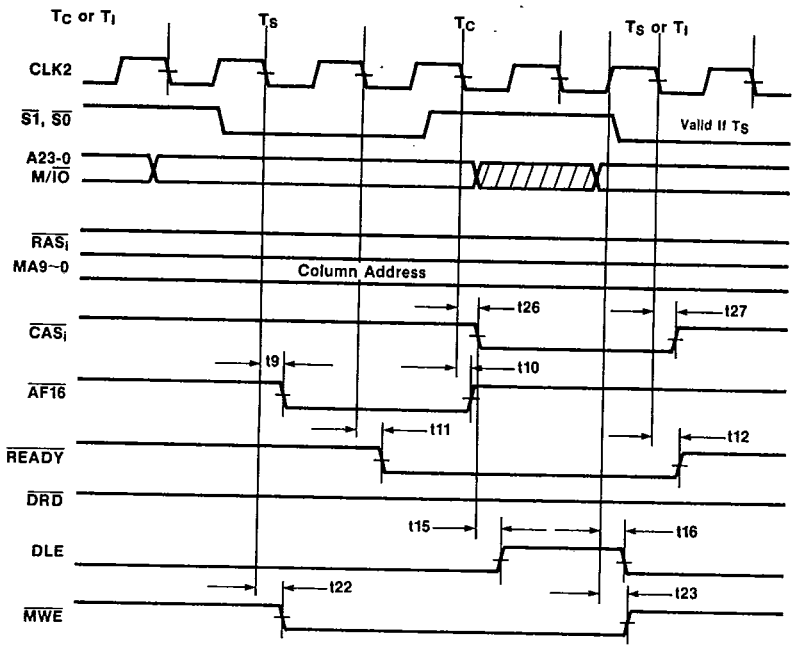

**Interleave Mode—Write Cycle with RAS Being Inactive, 0WS**

## 2.10 82C212 Timing Diagrams (Continued)



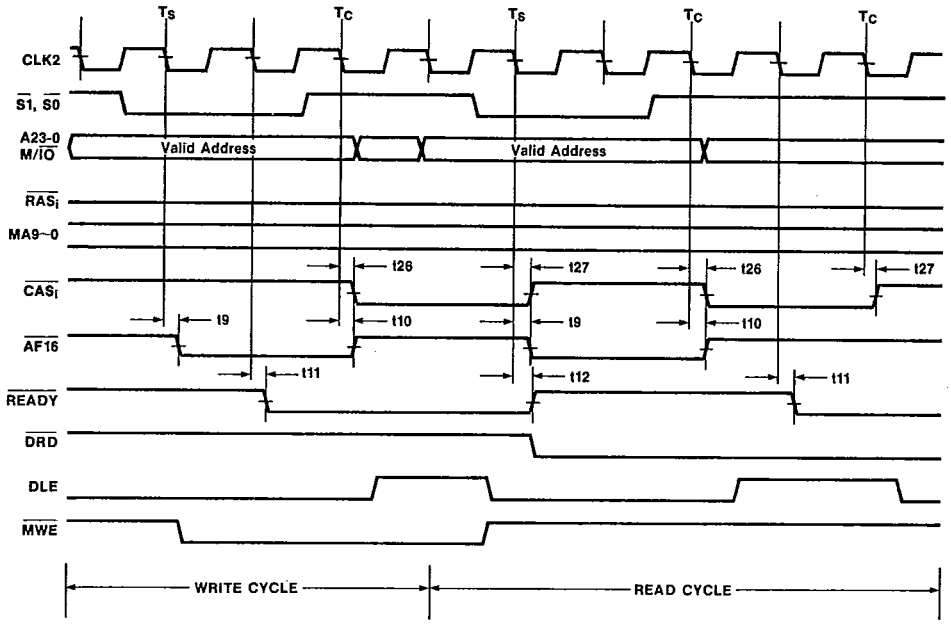

**Interleave Mode—Read Cycle with RAS Being Inactive, 0WS**

## 2.10 82C212 Timing Diagrams (Continued)




**Interleave Mode—Write, 0WS (RAS active)**

## 2.10 82C212 Timing Diagrams (Continued)




**Interleave Mode—Read After Write, 0WS (RAS active)**

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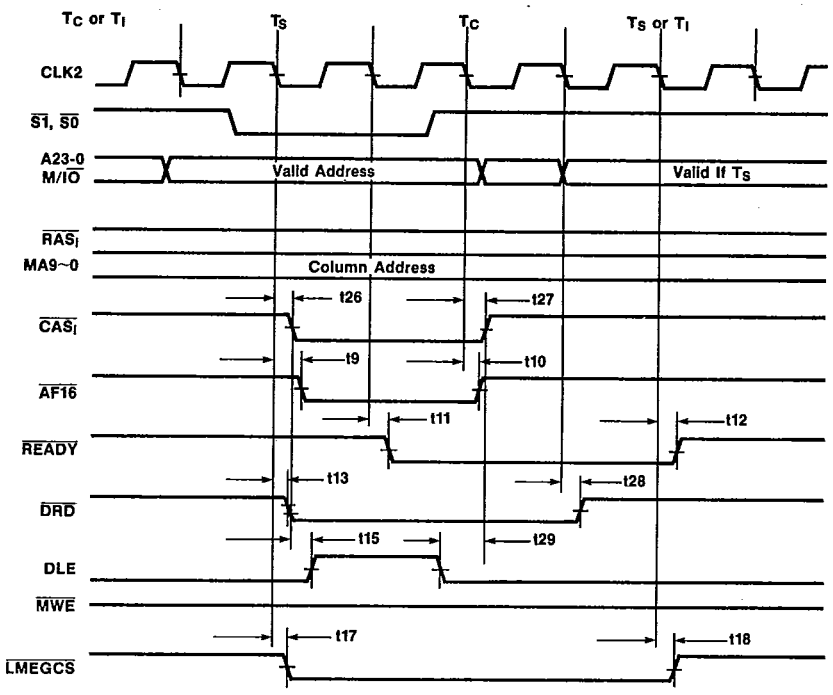
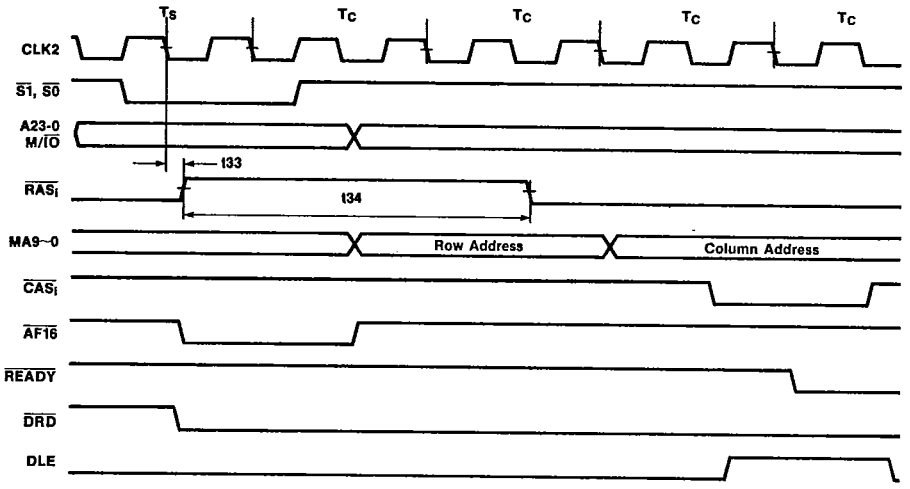
## 2.10 82C212 Timing Diagrams (Continued)



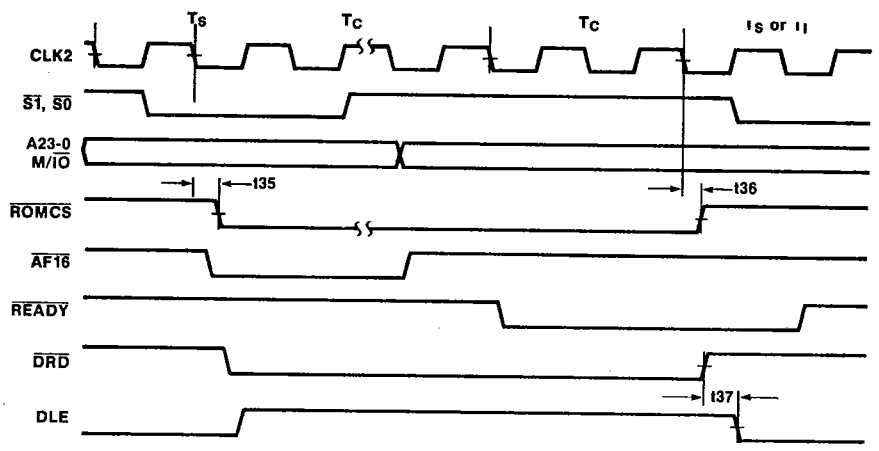

**Interlevae Mode—Read, 0WS (RAS active)**

## 2.10 82C212 Timing Diagrams (Continued)



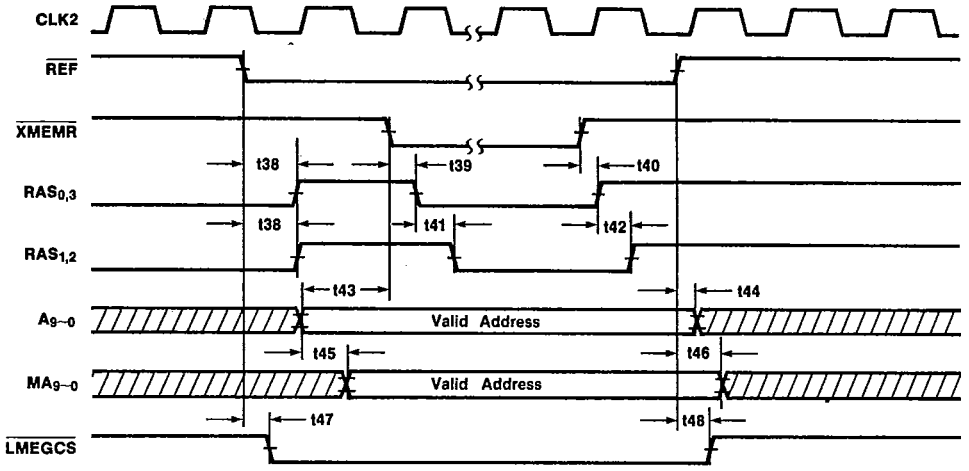

**Interleave Mode—Read Miss Cycle**

## 2.10 82C212 Timing Diagrams (Continued)



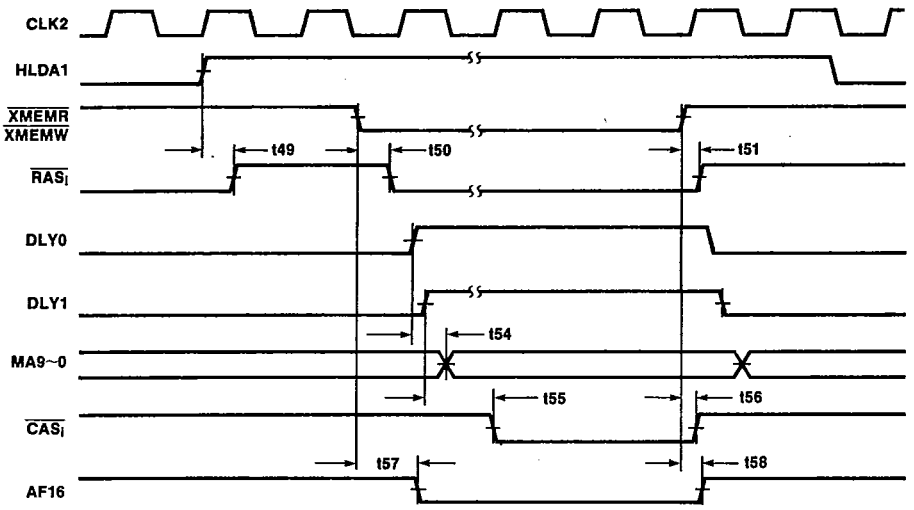

**ROM Read Cycle**

## 2.10 82C212 Timing Diagrams (Continued)




**Refresh Cycle**

## 2.10 82C212 Timing Diagrams (Continued)




DMA Cycle

# 3 82C215 DATA/ADDRESS BUFFER

## 3.1 Features

- Bus Conversion logic for 16 bit to 8 bit transfers
- Parity generation/detection logic

## 3.2 Functional Description

Figure 3.1 is a block diagram of the 82C215 Data/Address buffer. It consists of four modules:

- Address buffers and latches
- Data buffers and latches
- Bus conversion logic
- Parity generation/detection logic

### 3.2.1 Address Buffers and Latches

The 82C215 provides the address buffering between the CPU address lines A1-A16 and the XA1-XA16 lines. These buffers drive 4 mA output low currents ($I_{OL}$). The CPU address lines are latched by IALE to generate the X-Address lines when HLDA is inactive.

### 3.2.2 Data Buffers and Latches

The 82C215 provides the buffering between the CPU data bus (D0-D15) and the memory data bus (MD0-MD15). The D0-D15 lines drive 4 mA output low currents ($I_{OL}$). The MD0-MD15 lines drive 8 mA $I_{OL}$. The enable signal for the latch between the Memory Data bus and the CPU Data bus is controlled by $\overline{DRD}$, HLDA and the action codes. This allows 16 bit reads from 8 bit peripherals controlled by the 82C211.

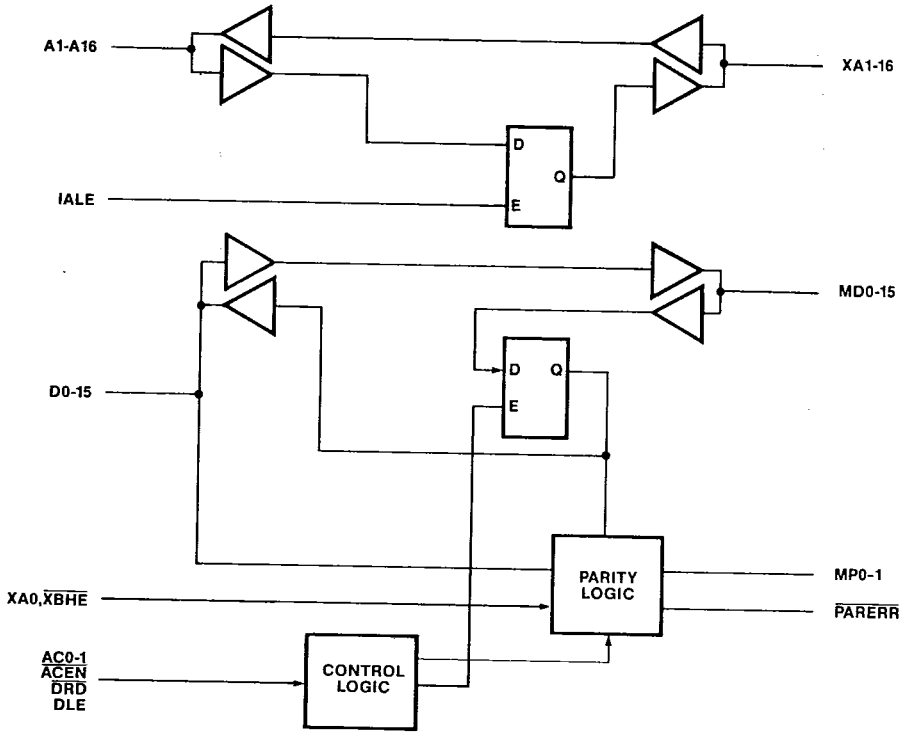



**Figure 3.1 82C215 Block Diagram**

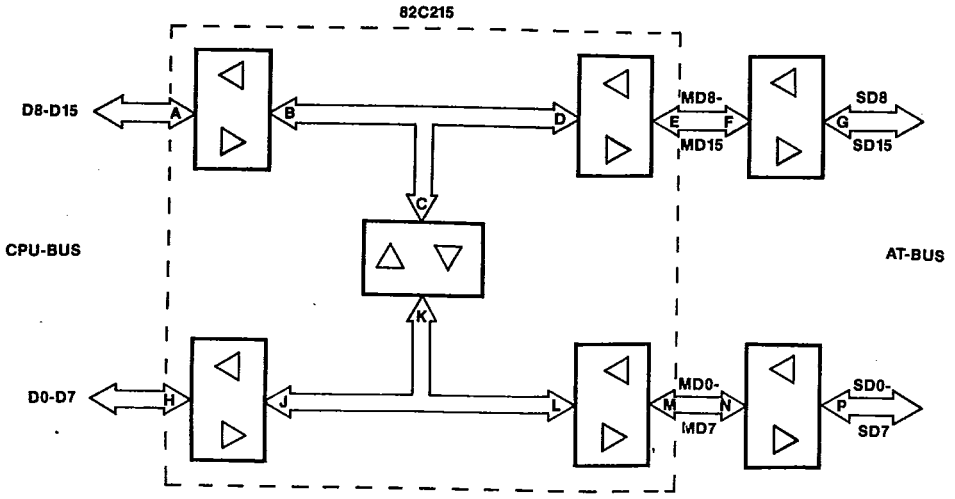



**Figure 3.2 Bus Conversion Data Paths**

### 3.3.3 Bus Conversion Logic

The 82C215 provides data bus conversion when the 16 bit CPU reads from or writes to 8 bit devices. It also provides bus conversion for Master/DMA cycles. There are six possible cases, as seen in Table 3.1 in conjunction with Figure 3.2. These conversions are controlled by the action codes which are qualified by $\overline{\text{ACEN}}$ from the 82C211.

### 3.3.4 Parity Generation/Detection Logic

For local RAM write cycles, the 82C215 generates even parity for each of the two bytes of the data word. These valid even parity bits are written to the parity bits MP0, MP1 in the local DRAMs. During a local memory read cycle, the 82C215 checks for even parity for each MD byte read. If the parity is detected as being odd, the 82C215 flags a parity error on the $\overline{\text{PARERR}}$ output line to the 82C211. The 82C211 distinguishes between local ROM and RAM cycles before sampling $\overline{\text{PARERR}}$.

Table 3.1

| AC1 | AC0 | Cycle | Operation | Data Path |
|---|---|---|---|---|
| 0 | 0 | CPU | 16 bit write | A-B-D-E-F-G and H-J-L-M-N-P |
| 0 | 0 | CPU | 8 bit LO write | H-J-L-M-N-P |
| 0 | 1 | CPU | 16 bit read | G-F-E-D-B-A and P-N-M-L-J-H |
| 0 | 1 | CPU | 8 bit LO read | P-N-M-L-J-H |
| 1 | 0 | CPU | 8 bit HI write | A-B-C-K-L-M-N-P |
| 1 | 1 | CPU | 8 bit HI read | P-N-M-L-K-C-B-A |
| 1 | 0 | DMA/MASTER | 8 bit HI write | P-N-M-L-K-C-D-E-F-G |
| 1 | 1 | DMA/MASTER | 8 bit HI read | G-F-E-D-C-K-L-M-N-P |

### 3.4 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | — | 7.0 | V |
| Input Voltage | $V_I$ | -0.5 | 5.5 | V |
| Output Voltage | $V_O$ | -0.5 | 5.5 | V |
| Operating Temperature | $T_{OP}$ | -25° | 85° | C |
| Storage Temperature | $T_{STG}$ | -40° | 125° | C |

**NOTE:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

### 3.5 82C215 Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.25 | V |
| Ambient Temperature | $T_A$ | 0° | 70° | C |

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### 3.6 82C215 DC Characteristics

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | — | 0.8 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | — | V |
| Output Low Voltage<br>$I_{OL}$ = 4mA | $V_{OL}$ | — | 0.45 | V |
| Output High Voltage<br>$I_{OH}$ = -4mA | $V_{OH}$ | 2.4 | — | V |
| Input Current<br>$0<V_{IN}<V_{CC}$ | $I_{IL}$ | — | ±10 | μA |
| Power Supply Current @ 16MHz | $I_{CC}$ | — | 80 | mA |
| Output High-Z Leakage Current<br>$0.45<V_{OUT}<V_{CC}$ | $I_{OZ1}$ | | ±10 | μA |
| Standby Power Supply Current | $I_{CCSB}$ | — | 1.0 | mA |

### 3.7 82C215-12, 82C215-16 AC Characteristics

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t1 | MD bus 3-stated after $\overline{DRD}$ active | 7.5 | | 24 | ns |
| t2 | MD bus valid to D bus valid | 8 | | 18.5 | ns |
| t3a | MD bus being driven after $\overline{DRD}$ inactive | 7.5 | | 28 | ns |
| t3b | MP0, MP1 being driven after $\overline{DRD}$ inactive | 6 | | 23 | ns |
| t4 | D bus invalid after $\overline{DRD}$ inactive | 4 | | 13 | ns |
| t5 | D bus 3-stated after $\overline{DRD}$ inactive | 6 | | 15 | ns |
| t6 | D bus valid to MD bus valid | 11 | | 19 | ns |
| t7 | D bus valid to MP1, MP0 valid | 11 | | 20 | ns |
| t8 | $\overline{ACEN}$ active to D bus valid | 16 | | 27 | ns |
| t9 | AC code valid to MD bus valid | 10 | | 19 | ns |
| t10 | AC code invalid to MD bus invalid | 11 | | 20 | ns |
| t11 | DLE inactive to $\overline{PARERR}$ enabled | 17 | | 30 | ns |
| t12 | $\overline{DRD}$ inactive to $\overline{PARERR}$ disabled | 17 | | 28 | ns |
| t13 | IALE active to XA bus valid | 11 | | 19 | ns |

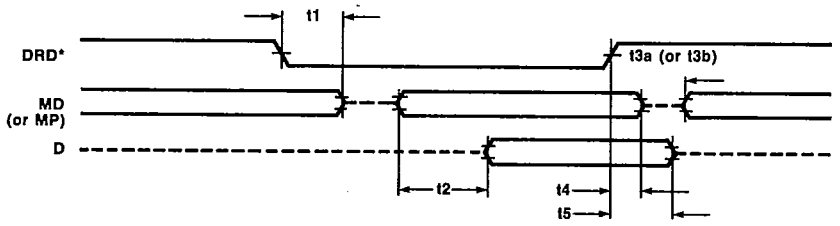
### 3.7 82C215-12, 82C215-16 AC Characteristics (Continued)

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

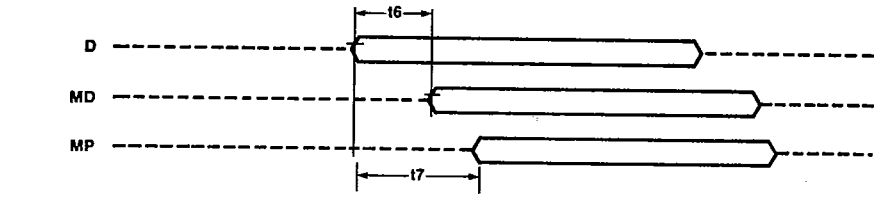
| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t14 | XA bus valid to A bus valid | 7 | | 16 (19) | ns |
| t15 | MD, MP setup time to DLE trailing edge | 0.0 | | | ns |
| t16 | MD, MP hold time from DLE trailing edge | 6.0 | | | ns |
| t17 | $\overline{DRD}$ setup time to DLE trailing edge | 12 | | | ns |
| t19 | MD bus hold time from $\overline{ACEN}$ trailing edge | 7.5 | | | ns |
| t20 | MD bus valid to MP valid during DMA memory write cycle | 14 | | 24 | ns |
| t21 | MD high byte valid to MD low byte valid during DMA high memory read cycle | 10 | | 19 | ns |
| t22 | AC code valid to MD high byte valid during DMA high memory write cycle | 9 | | 18 | ns |
| t23 | AC code valid to MP valid during DMA high memory write cycle | 17 | | 28 | ns |

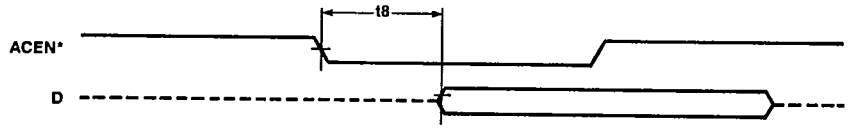
**Note:** Values inside ( ) are 12 MHz timing.

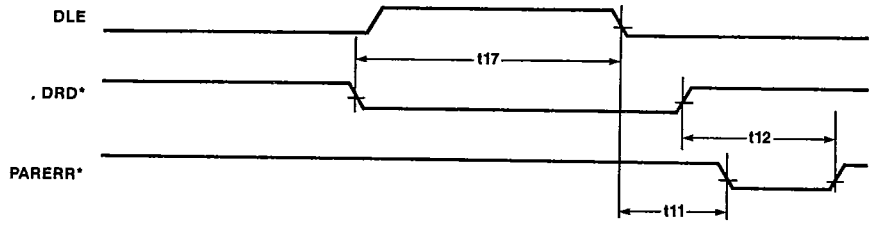
### 3.8 82C215 Timing Diagrams

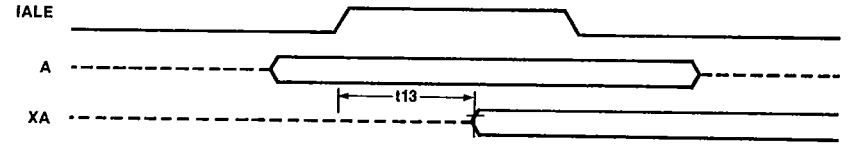


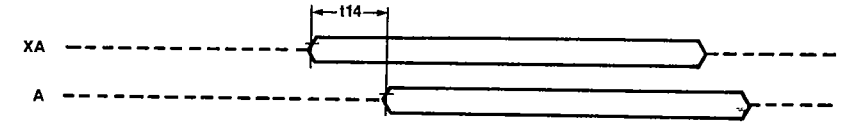
### 3.8 82C215 Timing Diagrams (Continued)



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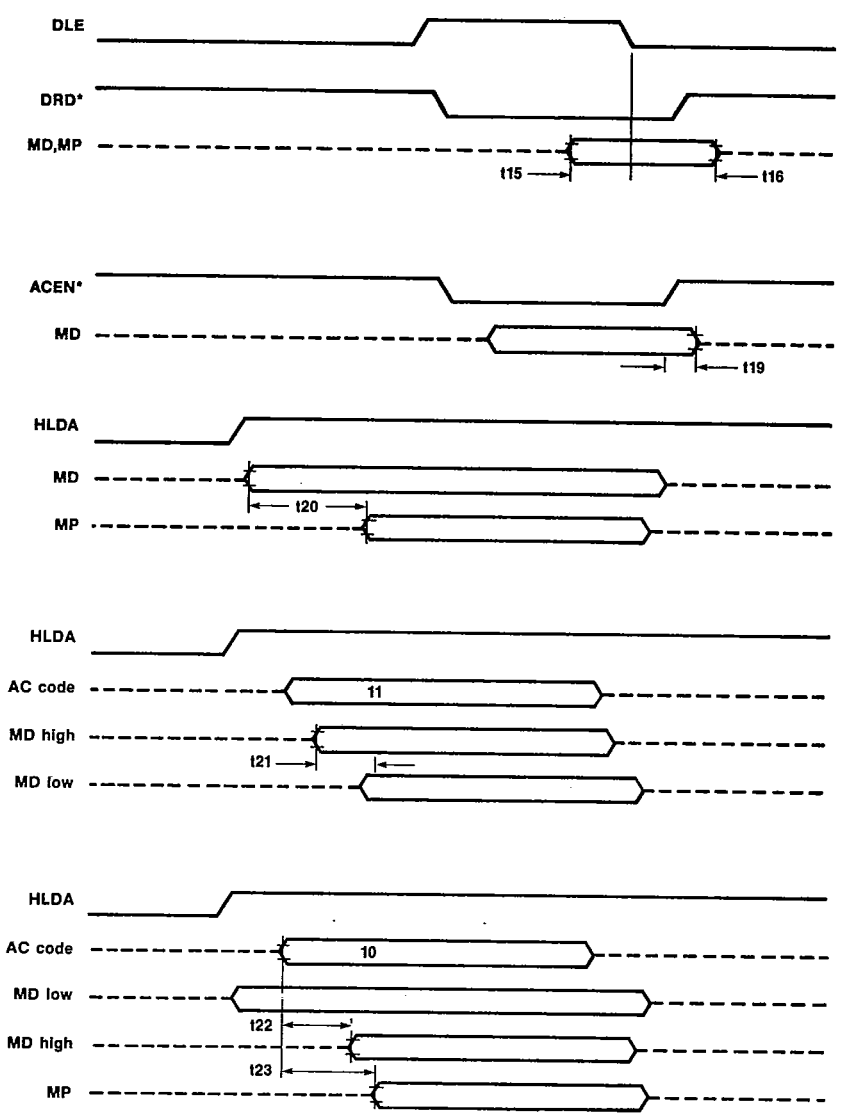
### 3.8 82C215 Timing Diagrams (Continued)



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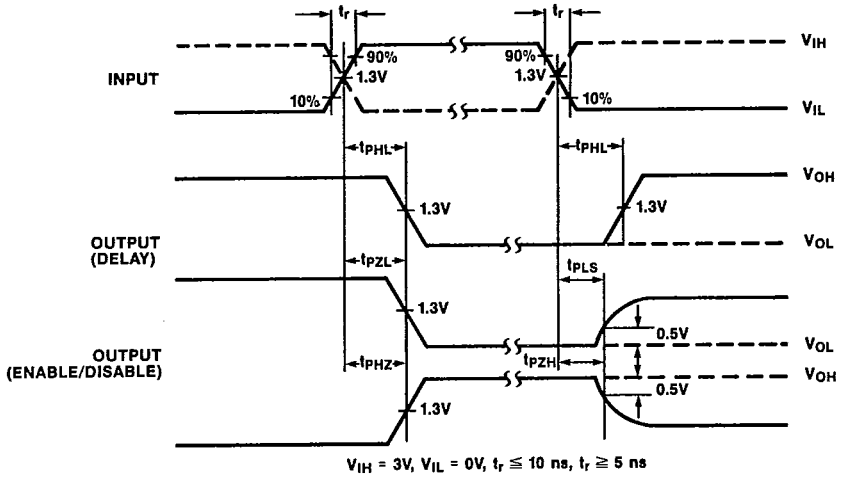
**Load Circuit Measurement Conditions**

| Parameter | Output Type | Symbol | $C_L$(pF) | $R_1$ (Ω) | $R_L$ (Ω) | $SW_1$ | $SW_2$ |
|---|---|---|---|---|---|---|---|
| Propagation Delay Time | Totem pole 3-state Bidirectional | $t_{PLH}$ $t_{PHL}$ | 50 | — | 1.0K | OFF | ON |
| Propagation Delay Time | Open drain or Open Collector | $t_{PLH}$ $t_{PHL}$ | 50 | 0.5K | — | ON | OFF |
| Disable Time | 3-state Bidirectional | $t_{PLZ}$ $t_{PHZ}$ | 5 | 0.5K | 1.0K | ON OFF | ON |
| Enable Time | 3-state Bidirectional | $t_{PZL}$ $t_{PZH}$ | 50 | 0.5K | 1.0K | ON OFF | ON ON |




$V_{IH}$ = 3V, $V_{IL}$ = 0V, $t_r \leqq 10$ ns, $t_r \geqq 5$ ns

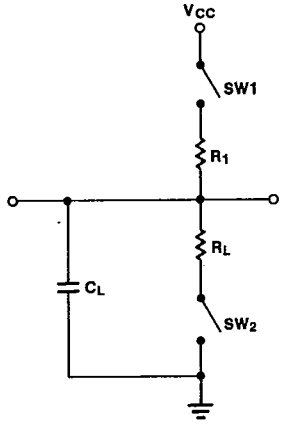



**Figure 10. Load Circuit and AC Characteristics Measurement Waveform**

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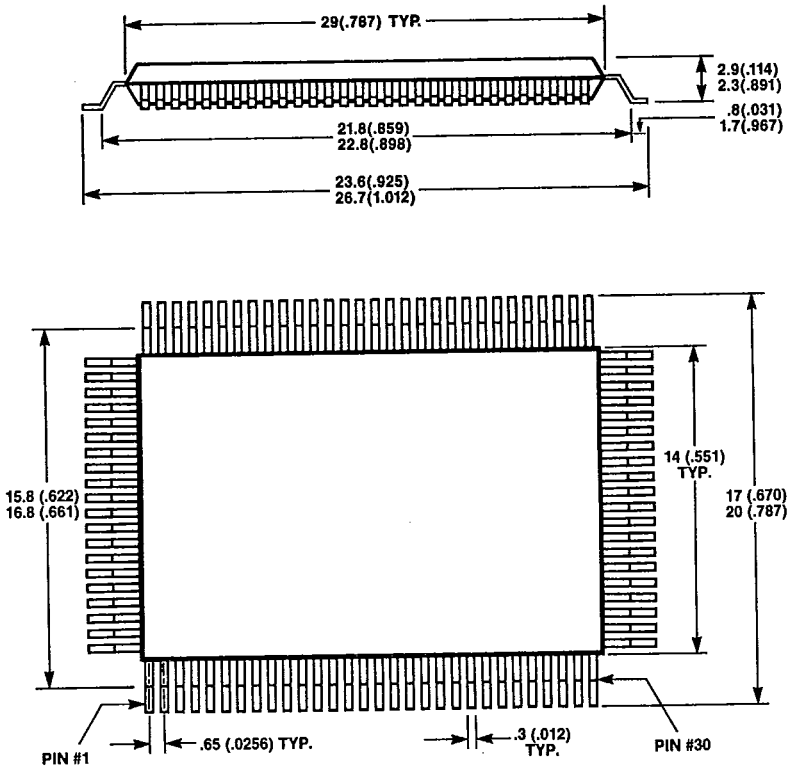
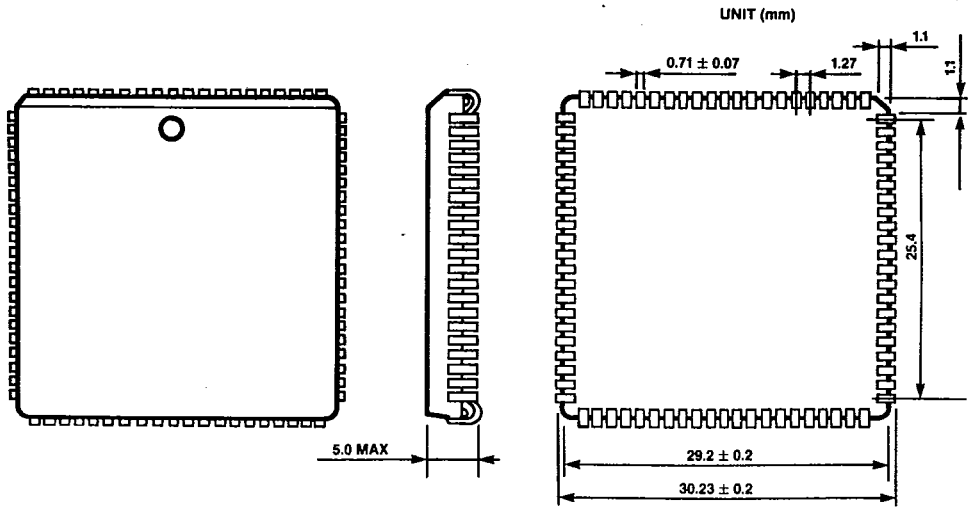
## 100-PIN PLASTIC FLAT PACKAGE




ALL DIMENSIONS IN MILLIMETERS (INCHES).

## 84-PIN PLASTIC LEADED CHIP CARRIER




### Ordering Information

| Order Number | Package Type |
|---|---|
| P82C211/212/215/206 | PLCC-84 pins |
| F82C211/212/215/206 | PFP-100 pins |

**Note:**
1. PLCC = Plastic Leaded Chip Carrier
   PFP = Plastic Flat Pack

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