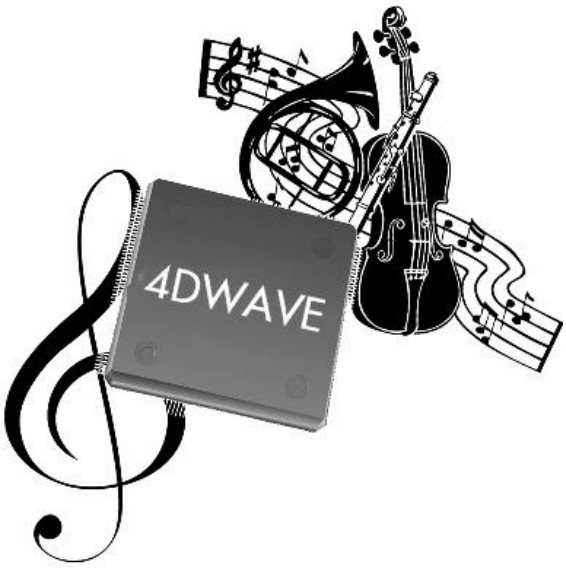
Trident 4DWAVE-DX Technical Reference Manual



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November 1997, Rev 0.2

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TRADEMARK ACKNOWLEDGMENTS

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1 Introduction

1.1 Advanced PCI DirectSound™ Accelerator

The 4DWAVE-DX is an advanced PCI audio accelerator providing full legacy compatibility, wavetable synthesis, DirectMusic™, DirectSound™, and DirectSound3D™ on a single chip for the high-performance, cost-sensitive consumer market. It supports full SoundBlaster™ compatibility and is fully PC97/PC98 compliant. It is named 4DWAVE as it adds time as the 4th dimension to its interactive 3D positional audio wave streams. The time element includes such effects processing as adding Doppler, Chorus, and Reverb effects on top of the 3D positional audio and wavetable streams.

The 4DWAVE-DX integrates a 64-voice wavetable engine with per voice effect processing capability. It supports the upcoming Microsoft® DirectMusic™ API and is fully compatible with the DLS Level 1 (downloadable samples) specification. The 4DWAVE-DX is optimized for Microsoft® Windows® 98 and Windows® NT™5.0 WDM streaming architecture with re-routable endpoint support. 4DWAVE-DX integrates DirectX™ 5 3D positional audio accelerator by incorporating QSound® Labs' QSoft3D™ technology. It includes DirectSound3D™ acceleration hardware for ITD (Interaural Time Difference), IID (Interaural Intensity Difference), Pan, Delay, and Doppler hardware.

VirtualFM™and VirtualGS™ technologies maintain SoundBlaster™ Pro/16 DOS games compatibility while improving gaming audio quality. The 4DWAVE-DX utilizes a Digital Enhanced Game Port, when coupled with a DirectInput™ driver, can save up to 12% of the CPU overhead nominally required by a conventional analog game port. The 4DWAVE-DX employs a high precision 26-bit digital mixer, providing an accurate 20-bit output and higher than 90dB signal-to-noise ratio when used with a high quality AC '97 codec.

The 4DWAVE-DX is designed with aggressive power management in mind as well. It is both ACPI-compliant and PCI Bus Power Management Interface (PPMI)-compliant. With a low power 3.3V process and a space conscious 100 LQFP package, the 4DWAVE-DX is well suited for Notebook systems as well.

The 4DWAVE-DX delivers an impressive combination of features and performance to end-users without burdening them on price. By combining PCI Bus Mastering for DirectSound™ acceleration, Hardware Wavetable synthesizer, Digital Enhanced Game Port, and interactive 3D positional audio acceleration through QSoft3D™, the 4DWAVE-DX provides up to a 40% system level performance enhancement over an equivalent ISA audio controller. It delivers high performance, high quality audio, high-end features with efficient power management in a single-chip in a space-efficient 100 LQFP package.

It is forward socket-compatible with future 4DWAVE family products. This document will briefly describe signals in future products to enable system designers to accommodate the future 4DWAVE family products with one design, substantially simplifying future design and testing efforts.

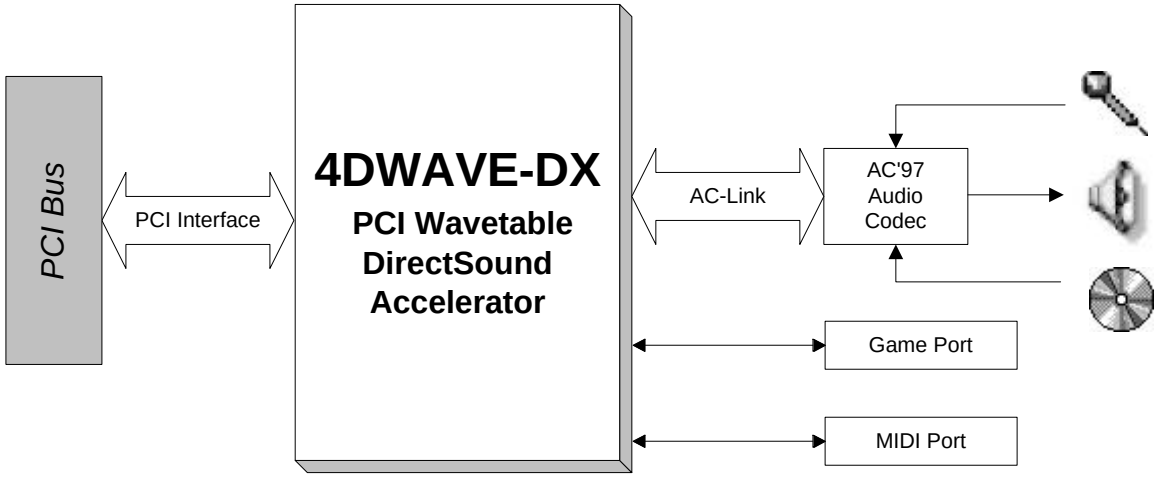


Figure 1-1. 4DWAVE-DX High Level System Block Diagram

1.2 Feature Highlights

1.2.1 Advanced PCI DirectSound Accelerator

- PCI 2.1-compliant with Bus Mastering optimized for multiple streams operation
- On-chip per voice cache minimizes PCI bandwidth
- Up to 20X improvement over ISA DMA on PCI bus bandwidth utilization
- Hardware multi-channel digital mixer

1.2.2 High Quality Wavetable Synthesizer

- 64 voices polyphony wavetable synthesizer supports all combinations wavetable samples formats :
  - Stereo/mono
  - 8-/16-bits
  - Signed/unsigned
- Per channel volume and envelope control, pitch shift, tremolo, and vibrato
- Per channel effect processing and effect volume control for reverb, chorus and echo
- Microsoft® DirectMusic™ support (upcoming) with unlimited downloadable samples in system memory
- DLS1-compliant Downloadable Samples support

1.2.3 Full Legacy and DOS Games Compatibility

- Legacy game audio support with SoundBlaster™ Pro/16 compatibility on the PCI bus
- Legacy DMA support on PCI Bus with DDMA-enabled or standard (non-DDMA) PCI chipsets
- VirtualFM™ enhances audio experience through real-time FM-to–wavetable conversion
- MPU-401 compatible UART for external or internal synthesis
- VirtualGS™ provides General MIDI/GS command interpretation for wavetable & effect synthesis

1.2.4 High Quality Audio and AC ’97 Support

- CD quality audio with better or equal to 90dB signal-to-noise ratio using an external high quality AC ’97 codec
- AC ’97 support with full duplex, independent sample rate converter for audio recording and playback
- On-chip sample rate converter ensures all internal operation at 48KHz
- High precision internal 26-bit digital mixer with 16- and 20-bit digital audio output

1.2.5 Advanced Streaming Architecture

- Microsoft® WDM Streaming architecture compliant and “Re-routable endpoint” support
- Three stereo capture channels
- AC ’97 stereo recording channel through AC-link

1.2.6 Microsoft® DirectSound™/DirectSound3D™ Support

- 64 voices DirectSound™ channels
- DirectSound3D™ accelerator with IID, ITD, and Doppler effects on 3D positional audio buffers
- DirectSound™ accelerator for volume, pan, and pitch shift control on streaming or static buffers
- QSound® QSoft3D™-based interactive 3D positional audio accelerator for DirectX™ 5

1.2.7 Extras

- Fully Plug and Play PCI controller and software
- Digital Enhanced Game port enables analog joystick to emulate digital joystick performance using Trident- provided DirectInput™ driver. This eliminates up to 12% of CPU overhead wasted on joystick polling.
- DirectX™ timer for video/audio synchronization
- Forward pin-compatible with next generation PCI audio accelerators

1.2.8 Software Support

- Complete DirectX™ driver suite (DirectSound3D™, DirectSound™, DirectMusic™, and DirectInput™) for Windows® 95 and Windows® 98/NT 5.0®
- Configuration, installation, and diagnostics under real mode DOS, Windows® 95/Windows® 98 DOS box
- Windows® 3.1, 95, NT4.0, Windows® 98/NT5.0 configuration, installation, and mixer program
- 2, 4, or 8 Mbytes General MIDI (GM)/General Sound (GS) compliant sample Library

1.2.9 Power Management

- Desktop ACPI & PPMI Compatible
- Software Controls AC '97 Codec Power States

1.2.10 Testability

- NAND Tree test mode
- Tri-state all I/Os test mode
- Loop-back modes for Diagnostics
- All Mixer Channels can be captured

1.2.11 Process

- Advanced 0.35um process
- Low power 3.3V (5V-safe) operation

1.2.12 Package and Ordering

- 100 LQFP (14mm x 14mm x 1.4mm)
- Ordering Part Number : 7700

1.3 Reference Documents

- PCI Local Bus Specification, Revision 2.1, June 1, 1995
- ACPI - Advanced Configuration and Power Interface Specification, Revision 1.0
- PPMI - PCI Bus Power Management Interface Specification, Revision 1.0, March 18, 1997
- OnNow - Device Class Power Management Reference Specification, Audio Device Class V1.0
- AC '97 - Audio Codec '97 Component Specification, Revision 1.03, September 15, 1996
- 8237A High Performance Programmable DMA Controller, October 1987
- DMA on the "PCIway", Revision 6.0
- SoundBlaster Programming Information - V0.90, January 29, 1995
- Developer Kit for SoundBlaster Series, 2nd Edition, October 1993

2 System and Architecture Overview

The 4DWAVE-DX is a 64-Voice PCI Wavetable/DirectSound™ Audio Accelerator. It is packaged in a 100-pin LQFP package targeted for desktop and space-constrained applications such as notebook or handheld computer design. As shown in Figure 1.1 above, the 4DWAVE-DX will interface to:

- PCI bus
- AC '97 serial bus for communication with an AC '97 Codec
- Digitally Enhanced Game Port
- MIDI port

The 4DWAVE family devices are designed to enable a single driver set to support current and future generation devices. This approach allows a stable, maintainable code base. The hardware/software combinations provide the following acceleration and functions:

- DirectSound™ acceleration
- 64-voice Wavetable synthesis
- Chorus effects
- Reverb effects
- FM Synthesis via VirtualFM™ technology
- General MIDI/GS command interpreter via VirtualGM™/VirtualGS™ technology
- 3D positional audio effects

Figure 1.2 shows the major functional blocks of the 4DWAVE-DX. The following sections provide architectural descriptions for each of the functional blocks.

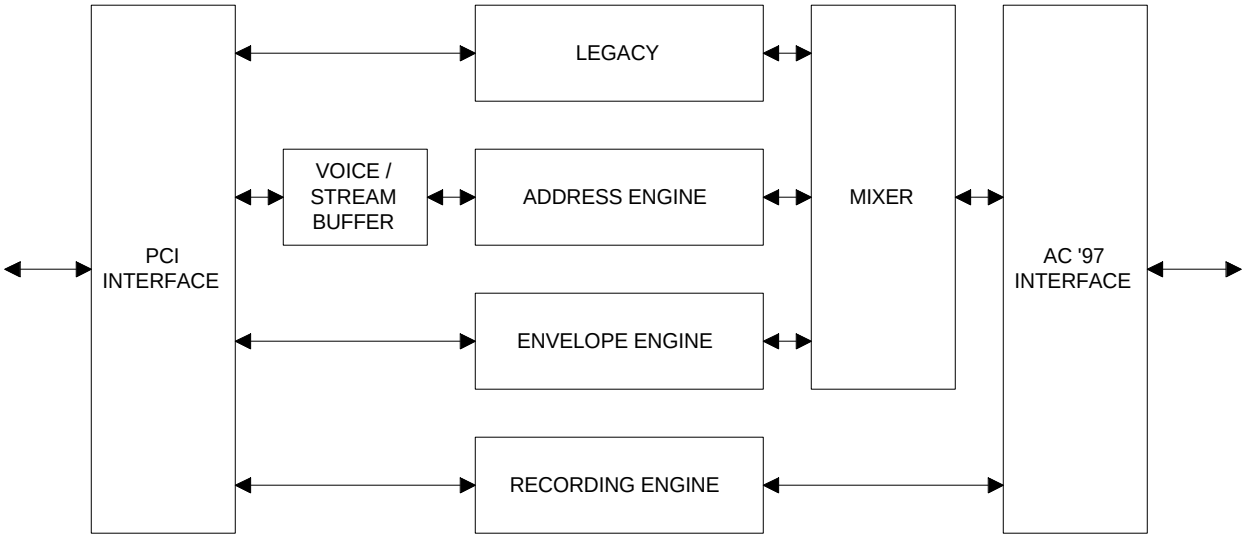


Figure 1-2. 4DWAVE-DX Functional Block Diagram

2.1 PCI Interface

The 4DWAVE-DX PCI interface is fully PCI Rev 2.1 and Plug-n-Play compliant. It consists of separate master and slave controllers that operate independently. Both master and slave engine support burst cycles. The slave can be programmed to accept both I/O and Memory (memory mapped I/O) cycles for 4DWAVE-DX registers. The 4DWAVE-DX register space can be mapped by configuring the PCI Configuration registers for I/O and Memory base addressing. The legacy register space is only accessible through I/O cycles and cannot be remapped.

4DWAVE-DX uses a single PCI interrupt. All interrupts are combined together internally to form this single interrupt signal. Internal registers must be accessed to determine the nature of the interrupt. This function is programmed differently if the device is in legacy emulation mode or not.

For emulation legacy DMA operation, the device can be configured to use either the Distributed DMA (DDMA, Rev 6.0 spec.) mechanism or a Trident proprietary DMA snooping mechanism depending on whether the system core logic supports Distributed DMA or not.

2.2 Legacy

The 4DWAVE-DX supports both the SoundBlaster™ Pro and SoundBlaster™ 16 register sets. This includes the Adlib, OPL3, MPU-401, and Game Port. When configured to support legacy operation, the device will respond to all I/O cycles in the legacy address regions. It integrates an on-chip SoundBlaster™ compatible command interpreter. The OPL3 and MPU-401 compatibility are handled by Trident's VirtualFM™ and VirtualGM™/VirtualGS™ technologies and are based on a hardware/software combination to provide the emulation of FM synthesis and General MIDI/GS command interpretation in DOS. The hardware provides all the registers for reads and writes to legacy locations while the software provides the interpretation and emulation.

The 4DWAVE-DX supports a legacy analog game port and Digitally Enhanced Game Port. When using with a bundled DirectInput™ driver, the Digitally Enhanced Game Port allows a dramatic reduction in both bus traffic and CPU utilization by removing the requirement of "I/O polling" for the joystick position. This can save up to 12% of CPU overhead; this substantially enhances game performance and the gaming experience. The MIDI port is supported with an MPU-401 compatible UART. This port can also be used in an emulation mode (VirtualGM™/VirtualGS™) to support synthesis in DOS mode games.

2.3 Voice Buffer/Stream Buffer

The voice buffer/stream buffer is used to buffer the data streams between the accelerator engine and the system memory. The stream buffer supports up to 64 channels with a 4 Dword-deep buffer per channel. The stream buffer is used for: (a) playback of up to 64 streams of audio and effects, and (b) to support three capture channels WDM, chorus, and reverb effects.

2.4 Address Engine

The address engine supports 64 voice channels. Stereo/mono, 8-/16-bit, and signed/unsigned formats are supported. All 64 voices are optimized for DirectX™/WDM audio streams. Each channel is sample rate converted to 48KHz. The address engine performs all the sample address calculations including using a channel specific sample rate conversion factor.

2.5 Envelope Engine

The envelope engine controls the channel volume. For the first 32 channels, it supports two global volumes, a per/channel volume, a left-right PAN, a chorus volume, and a reverb volume. The first set also includes two volume slope buffers to allow a MIDI ADSR (Attack-Decay-Sustain-Release) curve to be performed. The second 32 channels support a per/channel volume, a left-right PAN, a chorus volume, and a reverb volume. All volume controls operate in dBs (decibels) of attenuation. This allows the attenuations to simply be summed before sending the composite to the mixer.

2.6 Mixer

The 4DWAVE-DX digital mixer supports high-precision 26-bit accumulators on three separate stereo channels. The hi-resolution accumulation allows the 64 voices to be mixed (accumulated) without degradations such as "clipping". The mixer supports both 16-bit and 20-bit audio outputs, when coupled with high quality AC '97 codec, and can provide higher than 90dB signal-to-noise ratio.

There is a separate mixer channel for each of main (AC '97 stereo out), reverb, and chorus output. The main mixer channel data is buffered in a FIFO before being accessed by the AC '97 interface. This allows the device to buffer several samples ahead and substantially increases its tolerance for bus latency and others delays caused by other system events.

2.7 Recording Engine

The recording engine records data samples from the AC '97 codec. All AC '97 data is sampled at 48KHz and can be recorded in 16-bit stereo format. This requires 4-bytes per sample or 192Kbytes for 1 second of record data. The recording channel also supports independent down sampling and format conversion. By down sampling, the bus bandwidth and memory space can be reduced. For instance, voice function using 8-bit mono samples at 8KHz uses only 8K bytes per second.

2.8 AC '97 Interface

The AC '97 interface supports the 5-pin AC'Link interface to the codec. The AC '97 interface operates at a fixed 48KHz sample rate. It provides 20-bit stereo output for playback and supports 16-bit stereo input for recording. The interface also includes a register set that allows access to the external AC '97 codec registers. AC '97 power management and AC '97 cold and warm are fully supported.

3 Package and Pin Assignments

The 4DWAVE-DX is packaged in a space-efficient 100 pin LQFP package (14mm x 14mm x 1.4mm). The 4DWAVE-DX pins can be classified into five functional categories and one forward-compatible category:

- PCI Interface
- AC '97 Interface
- MIDI/Game Port Interface
- Test Logic
- Power/Ground
- Forward-Compatible signal group

3.1 Pin Assignment Table and Signal Description

The following legends are used for pin characteristics in the "Type" column in Sections 3.1.1 to 3.1.6.

I = Input	O = Output	T = Tri-state
PWR = Power	GND = Ground	PU = Internal Pull-Up

The "I/O Buffer" columns in Section 3.1.1 to 3.1.6 indicate the various I/O buffer/cells used in the 4DWAVE-DX. Table 3.1 shows the detailed I/O buffer characteristics for each I/O buffer type used.

Table 3-1. Detailed I/O Buffer Characteristics

I/O Cell	Pull-up	Voltage Level	Ioh (mA)	Iol (mA)	Voltage (V)
IBUFT_5S		TTL			5V safe
BT8_5S		TTL	8	8	5V safe
BT8OD_5S		TTL	8	8	5V safe
BT10U_5S	√	TTL	10	10	5V safe
BDT4U_5S	√	TTL	4	4	5V safe
BDT6U_5S	√	TTL	6	6	5V safe
BDT10U_5S	√	TTL	10	10	5V safe
BDT10_5S		TTL	10	10	5V safe
V5SFPAD					5V
VDD5SPAD					3.3V
VSS5SPAD					GND

3.1.1 PCI Interface

Pin Number(s)	Signal Name	Type	I/O Buffer	Signal Description
85-87,89-93, 97-99,2-6,20-24, 27-29,31, 33-37, 39-40	AD[31:0]	T/I/O	BDT10_5S	AD[31:0] (Address-Data) is the PCI 32-bit multiplexed address and data bus. It is used to transmit the address during the "command" phase and is used to send or receive data during the "data" phase.
95,8,18,30	C/BE[3:0]#	T/I/O	BDT10_5S	C/BE[3:0]# (Command/Byte Enable) is the PCI 4-bit multiplexed command and byte enable bus. It is used to transmit the command during the "command" phase and is used to send or receive the active low data byte enables during the "data" phase.
17	PAR	T/I/O	BDT10_5S	PAR (Parity) is even parity across AD[31:0] and C/BE[3:0]#. It is generated one clock after the address and data phases. The current master (delayed one clock) drives parity.
9	FRAME#	T/I/O	BDT10_5S	FRAME# (Cycle Frame) is driven by the current master active low to indicate the beginning of a transaction. It also can be held low to indicate that the master desires a multiple data transaction.
11	TRDY#	T/I/O	BDT10_5S	TRDY# (Target Ready) is driven by the current target active low to indicate it is ready to complete the current data phase.
10	IRDY#	T/I/O	BDT10_5S	IRDY# (Initiator Ready) is driven by the current master active low to indicate it is ready to complete the current data phase.
14	STOP#	T/I/O	BDT10_5S	STOP# (Stop) is driven by the current target to indicate that it desires to stop the current transaction.
12	DEVSEL#	T/I/O	BDT10_5S	DEVSEL# (Device Select) is driven active low by the addressed target to indicate that it is the target of the current transaction.
96	IDSEL	In	IBUFT_5S	IDSEL (Initialization Device Select) is an active high signal driven by the system logic to select a device during a configuration transaction.
16	SERR#	T/O	BDT10_5S	SERR# (System Error) is an active low signal that is used to signal the system of parity (data or address) or other system errors.
15	PERR#	T/O	BDT10_5S	PERR# (Parity Error) is an active low signal that is used to signal the system of only data parity errors.
84	REQ#	T/O	BT8_5S	REQ# (Request) is an active low signal that is driven by a master when it needs to request the bus for a transaction.
83	GNT#	In	IBUFT_5S	GNT# (Grant) is an active low signal that is driven by the system arbitration logic to signal a master that it has been granted the bus.
77	INTA#	T/O	BT8OD_5S	INTA# (Interrupt "A") is an asynchronous active low signal used to signal the processor/OS of an event that requires handling.

(Continued on next page)

PCI Interface (Cont'd)

Pin Number(s)	Signal Name	Type	I/O Buffer	Signal Description
80	RST#	In	IBUFTS_5S	RST# (Reset) is the PCI reset signal. It is an active low signal. This signal may be asynchronous to CLK. It bring the PCI sequencer and the PCI outputs to a known and defined state. The AC '97 reset control AC_RESET# will also be activated.
81	CLK	In	IBUFT_5S	CLK (Clock) is the PCI Bus operation clock. This clock is used as a reference for all bus transactions and is used by the audio engine as the operational clock.

3.1.2 AC '97 Interface

Pin Number(s)	Signal Name	Type	I/O Buffer	Signal Description
49	AC_SYNC	T/O	BDT6U_5S	AC_SYNC (AC '97 Sync) is used as a fixed 48kHz synchronization signal.
53	AC_BITCLK	In	IBUFT_5S	AC_BITCLK (AC '97 Bit Clock) is a 12.288MHz clock used for serial data transfer between the AC '97 and 4DWAVE-DX.
54	AC_SDATA_OUT	T/O	BDT6U_5S	AC_SDATA_OUT (AC '97 Serial Data Out) is the serial, time division multiplexed, AC '97 output data stream.
52	AC0_SDATA_IN	In	IBUFT_5S	AC0_SDATA_IN (Primary AC '97 Serial Data IN) is the serial, time division multiplexed, AC '97 input data stream. (Note : AC0 is used to differentiate with future secondary codecs such as AC1, AC2, etc. in multiple AC '97 support.)
48	AC_RESET#	T/O	BDT6U_5S	AC_RESET# (AC '97 Reset) is the active low master reset signal. This signal is controlled by the PCI RST# signal and the internal Power Management register.

3.1.3 MIDI/Game Port

Pin Number(s)	Signal Name	Type	I/O Buffer	Signal Description
55	MIDI_OUT	T/O	BT10U_5S	MIDI_OUT (MIDI Out) is the MIDI UART serial output signal.
56	MIDI_IN	In	IBUFT_5S	MIDI_IN (MIDI In) is the MIDI UART serial input signal.
58-61	GAMEH[3:0]	In	IBUFT_5S	GAMEH[3:0] is the MS-nibble of the Game Port. This nibble reads the Button values and is input only.
62,64-66	GAMEL[3:0]	T/I/O	BDT10U_5S	GAMEL[3:0] is the LS-nibble of the Game Port. This nibble "fires" the game port timer and applications can poll the current position by reading GAMEL[3:0] or through the Enhanced Game Port Position Register 1 & 2.

3.1.4 Test Logic

Pin Number(s)	Signal Name	Type	I/O Buffer	Signal Description
67,68	TEST[1:0]#	In PU	BDT4U_5S	TEST[1:0]# are the inputs that enable the 4DWAVE-DX into test modes during a low-to-high RST# transition. 0 0 reserved 0 1 Global Tristate 1 0 NAND Tree test 1 1 Normal Operation
70	TDO	T/O	BDT4U_5S	Test Data Out is the data out for the NAND Tree test mode.

3.1.5 Power

Pin Number(s)	Signal Name	Type	I/O Buffer	Signal Description
7	VCC_5V	Power	V5SFPAD	5V I/O Power for 5V Safe (Tolerant) Pads
1,19,26,38,51, 57,69,76,88	VCC	Power	VDD5SPAD	Power (3.3V)
13,25,32,44, 50,63,75,82, 94,100	VSS	Power	VSS5SPAD	Ground

3.1.6 Forward-Compatible Signal Group

These pins are not "No Connects" in 4DWAVE-DX and are defined for future socket-compatible 4DWAVE family products. Trident will provide applications notes and design assistance for system designs intended to accommodate future 4DWAVE family products in the same socket. These pins are shown as "shaded" pins in Section 3.2, Pin Assignment Diagram.

Pin Number(s)	Signal Name	Type	I/O Buffer	Signal Description
79	CLKRUN#	I/O	TBD	CLKRUN# (Clock Running) is an active low signal that controls whether the PCI clock may be stopped or should be kept running. This pin is intended for Notebook and "motherboard" design as CLKRUN# is not available on PCI slot.
78	PME#	I/O	TBD	PME# (Power Management Event) is an active low signal that informs the system core logic that an event has occurred that requires a modification to the power management state of the system. This pin is intended for Notebook and "motherboard" design as PME# is not available on PCI slot.
42	ROM_DATA	I/O	TBD	Serial ROM Data signal. This pin should be connected to the "data" pin of a 2-pin serial EEPROM.
41	ROM_CLK	I/O	TBD	Serial ROM transfer clock. This pin should be connected to the "clock" pin of a 2-pin serial EEPROM.
46	I2S_SCLK	In	TBD	I^2S serial bit clock. This pin is intended for Notebook design and should be connected to the ZV-port SCLK pin.
45	I2S_LRCLK	In	TBD	I^2S word select; 0 = Left Word; 1 = Right Word. This pin is intended for Notebook design should be connected to the ZV-port LRCLK pin.
43	I2S_SDATA	I/O	TBD	I^2S: Serial Data In. This pin is intended for Notebook design and should be connected to the ZV-port SDATA pin.
47	AC1_SDATA_IN	In	TBD	AC1_SDATA_IN Secondary AC '97 serial data in. This pin should be connected to the secondary AC '97 Rev 2.0 codec as recommended by AC '97 Rev 2.0 spec.
74	XVSS	In	TBD	Crystal Ground
71	XVCC	In	TBD	Crystal Power
72	XTALI	In	TBD	Crystal Input
73	XTALO	In	TBD	Crystal Output

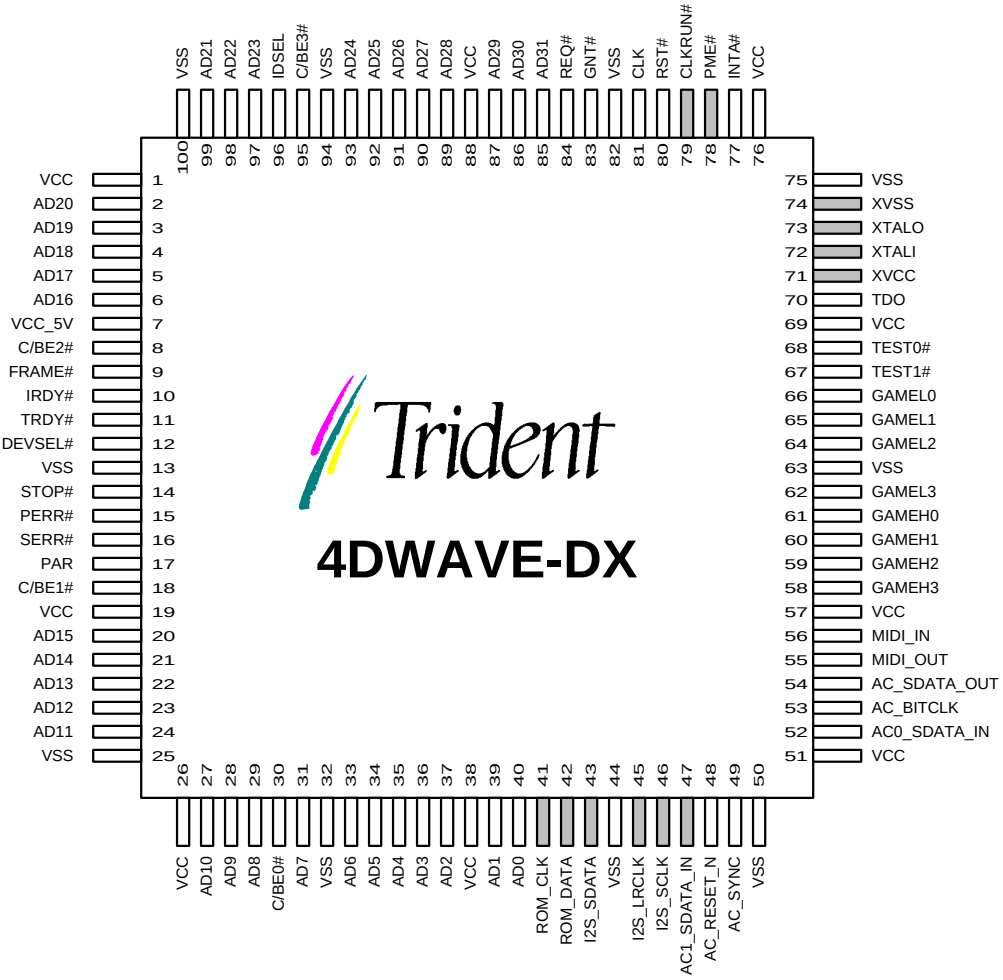
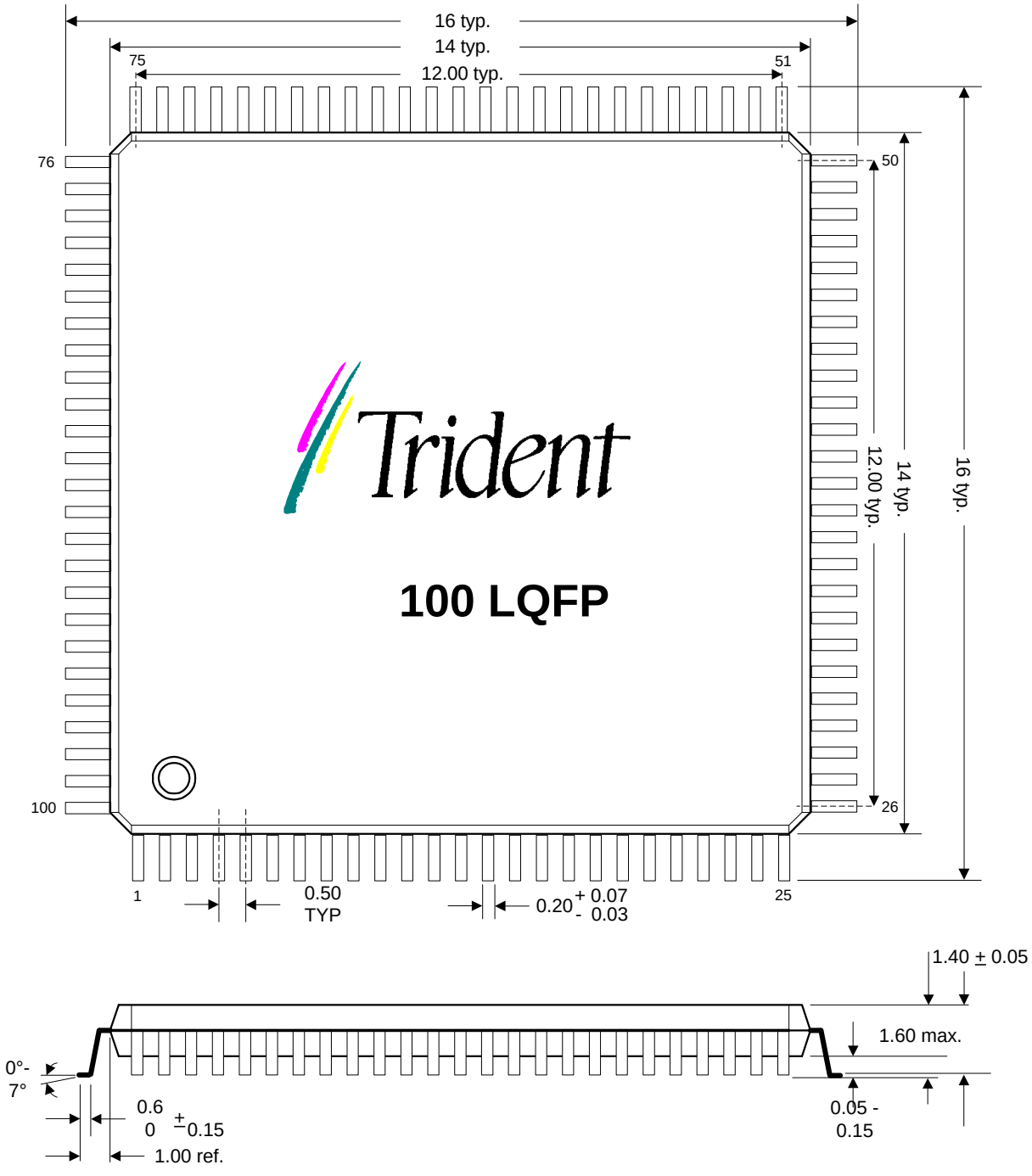


Figure 3-1. 4DWAVE-DX Pin Assignment

Note: The shaded pins are not functional signals in 4DWAVE-DX and belong to the “Forward-compatible Signal Group” for future socket-compatible 4DWAVE family products. Refers to Section 3.1.6 for more details.

3.2 Physical Dimensions (mm)



4 Address Map and Register Description

The 4DWAVE-DX is a standalone single function PCI audio device. It has registers in three address spaces: PCI Configuration Header 0 space, I/O Space, and Memory Space. These spaces are initialized through Plug-n-Play system software routines by configuring the registers in the 256-byte PCI Configuration Register space.

The 4DWAVE-DX has three major groups of registers and are described in the following sections :

Section 4.1 PCI Configuration Registers

Section 4.2 Wave Engine and Control Registers

Section 4.3 Legacy Registers (SoundBlaster™, Adlib, MPU-401, Game Port)

4.1 PCI Configuration Space

The device is both PPMI and DDMA compatible, which requires additional registers for set-up. The Cap_Ptr points to offset 48h where additional registers defines the power management capabilities of 4DWAVE-DX.

Table 4-1. 4DWAVE-DX PCI Configuration Register Space

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
00h	Device ID (Read Only = 2000h)		Vendor ID (Read Only = 1023h)	
04h	Status		Command	
08h	Class Code (Read Only = 040100h)			Revision ID (Read Only = 00h)
0Ch	BIST (Read Only = 0000h)	Header Type (Read Only = 00h)	Latency Timer	Cache Line Size (Read Only = 0000h)
10h	Audio IO Base Address Register			
14h	Audio Memory Base Address Register			
18-28h	RSVD (Read Only = 00000000h)			
2Ch	Subsystem ID (Read Only = 2000h)		Subsystem Vendor ID (Read Only = 1023h)	
30h	RSVD (Read Only = 00000000h)			
34h	RSVD (Read Only = 000000h)			Cap_Ptr (Read Only = 48h)
38h	RSVD (Read Only = 00000000h)			
3Ch	MAX_LAT (Read Only = 05h)	MIN_GNT (Read Only = 02h)	Interrupt Pin (Read Only = 01h)	Interrupt Line
40h	DDMA_CFG			
44h	RSVD (Read Only = 00h)	LEGACY_CTRL	LEGACY_DMA	LEGACY_IOBASE
48h	Power Management Capabilities (Read Only = 0601h)		Next_Ptr (Read Only = 00h)	Cap_ID (Read Only = 01h)
4Ch	Power Value Data (Read Only = 00h)	PMCSR_BSE (Read Only – 00h)	Power Management Control/Status	
50h	RSVD (Read Only = 0000h)		Interrupt Snooping Control	

4.1.1 PCI Configuration Registers Description

4.1.1.1 Vendor ID (Offset = 00h)

Bits	POR	Read/Write	Description
[15:0]	1023h	R	Trident Microsystems' PCI Vendor ID

4.1.1.2 Device ID (Offset = 02h)

Bits	POR	Read/Write	Description
[15:0]	2000h	R	4DWAVE-DX Device ID

4.1.1.3 Command (Offset = 04h)

Bits	POR	Read/Write	Description
[15:10]	000000b	R	Reserved
[9]	0	R	Fast Back-to-Back enable for master transactions. The 4DWAVE-DX does not support this feature. This bit is hardwired to a '0'.
[8]	0	R/W	SERR# enable 0 = Disables the SERR# Driver 1 = Enables the SERR# Driver
[7]	0	R	Address/Data stepping or Wait cycle control. The 4DWAVE-DX does not support this feature. This bit is hard wired to a '0'.
[6]	0	R/W	Parity Enable 0 = Ignores parity errors. 1 = Report parity errors.
[5]	0	R	VGA palette snoop. The 4DWAVE-DX does not support this feature. This bit is hard wired to a '0'.
[4]	0	R	Enable the "Memory Write and Invalidate" command. The 4DWAVE-DX does not support this feature. This bit is hard wired to a '0'.
[3]	0	R	Enable the device to monitor Special Cycle commands. The 4DWAVE-DX does not support this feature. This bit is hard wired to a '0'.
[2]	0	R/W	Bus Master Enable 0 = Disables the Bus Master Operation 1 = Enables the Bus Master Operation
[1]	0	R/W	Memory Space Enable 0 = Disables the device to respond to Memory Space cycles 1 = Enables the device to respond to Memory Space cycles
[0]	0	R/W	I/O Space Enable 0 = Disables the device to respond to I/O Space cycles 1 = Enables the device to respond to I/O Space cycles

4.1.1.4 Status (Offset = 06h)

Bits	POR	Read/Write	Description
[15]	0	R/W 1 to Clear	Parity Error Detected. The device sets this bit, whenever it detects a parity error, even when the Command bit [6] is disabled.
[14]	0	R/W 1 to Clear	SERR# status. Set whenever this device asserts SERR#.
[13]	0	R/W 1 to Clear	Received Master-Abort status. Set whenever a transaction to this device is terminated with a Master-Abort.
[12]	0	R/W 1 to Clear	Received Target-Abort status. Set whenever a transaction by this device is terminated with a Target-Abort.
[11]	0	R	Signaled Target-Abort status. Set whenever a transaction to this device is terminated with a Target-Abort. This will never happen on 4DWAVE-DX.
[10:9]	01b	R	DEVSEL Timing. The device supports “Medium” DEVSEL timing.
[8]	0	R/W 1 to Clear	Data Parity Error Detected. This bit is set by the Master device when 1) it detects a data parity error, 2) it is the current Master, and 3) when the Command bit [6] is enabled to report parity errors.
[7]	0	R	Capable of Fast Back-to-Back cycles. The 4DWAVE-DX does not support this feature. This bit is hard wired to a ‘0’.
[6]	0	R	User Definable Features. The 4DWAVE-DX does not support this feature. This bit is hard wired to a ‘0’.
[5]	0	R	66MHz Capable. The 4DWAVE-DX does not support this feature. This bit is hard wired to a ‘0’.
[4]	1	R	Capabilities List. The 4DWAVE-DX supports “New Capabilities” structure.
[3:0]	0000b	R	Reserved

4.1.1.5 Revision ID (Offset = 08h)

Bits	POR	Read/Write	Description
[7:0]	00h	R	4DWAVE-DX Revision. First revision = 00h.

4.1.1.6 Class Code (Offset = 10h)

Bits	POR	Read/Write	Description
[23:16]	04h	R	Base Class. Multimedia = 04h
[15:8]	01h	R	Sub Class. Audio = 01h
[7:0]	00h	R	Interface Class. None Defined = 00h

4.1.1.7 Cache Line Size (Offset = 0Ch)

Bits	POR	Read/Write	Description
[7:0]	00h	R	Cache Line Size. The 4DWAVE-DX does not support this feature. This bit is hardwired to a '0'.

4.1.1.8 Latency Timer (Offset = 0Dh)

Bits	POR	Read/Write	Description
[7:3]	00000b	R/W	Latency Timer in 8-PCI Clock increments.
[2:0]	000b	R	Latency Timer LS 3-bits. Always 000b. This forces the latency to be incremented by 8-PCI Clocks at a time.

4.1.1.9 Header Type (Offset = 0Eh)

Bits	POR	Read/Write	Description
[7]	0	R	Multi-function device enable. The 4DWAVE-DX is not a multi-function device.
[6:0]	0000000b	R	Header Layout. The 4DWAVE-DX uses a "standard" configuration layout.

4.1.1.10 BIST (Offset = 0Fh)

Bits	POR	Read/Write	Description
[7:0]	00h	R	The 4DWAVE-DX does not support this feature. These bits are hardwired to a '00h'.

4.1.1.11 I/O Base Address (Offset = 10h)

Bits	POR	Read/Write	Description
[31:8]	000000h	R/W	I/O Base Address [31:8]. Specifies the MS 24-bits of the Audio I/O base address.
[7:2]	000000b	R	I/O Base Address [7:2]. Forces alignment to a 256-byte block.
[1]	0	R	Reserved.
[0]	1	R	I/O Base identifier.

4.1.1.12 Memory Base Address (Offset = 14h)

Bits	POR	Read/Write	Description
[31:12]	00000h	R/W	Memory Base Address [31:12]. Specifies the MS 20-bits of the Audio Memory base address.
[11:4]	00h	R	Memory Base Address [11:4]. Forces alignment to a 4K-byte block.
[3]	0	R	Prefetchable. The 4DWAVE-DX uses this space for Memory mapped I/Os. This is not a prefetchable or mergeable address space.
[2:1]	00b	R	Type. This can be located anywhere in 32-bit address space.
[0]	0	R	Memory Base identifier.

4.1.1.13 Subsystem Vendor ID (Offset = 2Ch)

Bits	POR	Read/Write	Description
[15:0]	1023h	R/(W)	Trident Microsystems's PCI Vendor ID is used as the default. This register can be written if bit [1] in PCI Config [46h] is enabled.

4.1.1.14 Subsystem ID (Offset = 2Eh)

Bits	POR	Read/Write	Description
[15:0]	2000h	R	The 4DWAVE-DX does not support this feature. These bits are hardwired to a '2000h'.

4.1.1.15 Capabilities Pointer (Offset = 34h)

Bits	POR	Read/Write	Description
[7:0]	48h	R	Capabilities Pointer. Absolute offset to the start of the extended capabilities configuration space.

4.1.1.16 Interrupt Line (Offset = 3Ch)

Bits	POR	Read/Write	Description
[7:0]	00h	R/W	Interrupt Line. This is used by the driver and Plug-n-Play setup code to identify the interrupt used by this device.

4.1.1.17 Interrupt Pin (Offset = 3Dh)

Bits	POR	Read/Write	Description
[7:0]	01h	R	Interrupt Pin. This is used to tell what pin the device uses. The 4DWAVE-DX uses the INTA# pin.

4.1.1.18 Minimum Grant (Offset = 3Eh)

Bits	POR	Read/Write	Description
[7:0]	02h	R	Minimum Latency. The minimum time to complete a burst is 500ns. (2 x 0.25us increment)

4.1.1.19 Maximum Latency (Offset = 3Fh)

Bits	POR	Read/Write	Description
[7:0]	05h	R	Maximum Latency. The maximum time between request cycles is set at 1.25us (5 x 0.25us increment)

4.1.2 Legacy Configuration Registers Description

4.1.2.1 Distributed DMA Configuration (Offset = 40h)

Bits	POR	Read/Write	Description
[31:4]	0000000h	R/W	DDMA Base Address [31:4]
[3]	0	R/W	Non Legacy Extended Addressing Control (Fully 32 bit Addressing) 0 = disabled 1 = enabled
[2:1]	00b	R	Legacy DMA Transfer Size Control 00 8 bit transfer, legacy
[0]	0	R/W	DDMA Slave Channel Access Enable Control 0 = disabled 1 = enabled

4.1.2.2 Legacy I/O Base (Offset = 44h)

Bits	POR	Read/Write	Description
[7]	0	R/W	MPU-401 Legacy Address Space Enable 0 = MPU401Base disable 1 = MPU401Base enable
[6]	0	R/W	MPU-401 Legacy Address Space Select 0 = MPU401Base 0330h-0333h 1 = MPU401Base 0300h-0303h
[5]	0	R/W	Game Port Legacy Address Space Enable 0 = GAMEBase disable 1 = GAMEBase enable
[4]	0	R/W	Game Port Legacy Address Space Select 0 = GAMEBase 0200h-0207h 1 = GAMEBase 0208h-020Fh
[3]	0	R/W	Adlib Legacy Address Space Enable 0 = ADLIBBase disable 1 = ADLIBBase enable
[2]	0	R/W	Adlib Legacy Address Space Select 0 = ADLIBBase 0388h-038Bh 1 = ADLIBBase 038Ch-038Fh
[1]	0	R/W	SoundBlaster™ Legacy Address Space Enable 0 = SBBase disable 1 = SBBase enable
[0]	0	R/W	SoundBlaster™ Legacy Address Space Select 0 = SBBase 0220h-022Fh 1 = SBBase 0240h-024Fh

4.1.2.3 Legacy DMA (Offset = 45h)

Bits	POR	Read/Write	Description
[7:4]	0h	R	Reserved
[3]	0	R	Reserved
[2]	0	R	Reserved
[1]	0	R/W	Enable Legacy DMA Snooping/Trapping 0 = DMA trapping disable 1 = DMA trapping enable
[0]	0	R/W	DMA Snooping Channel Select 0 = DMA channel 1 trapping 1 = DMA channel 0 trapping

4.1.2.4 Legacy Control (Offset = 46h)

Bits	POR	Read/Write	Description
[7:3]	00000b	R/W	Reserved
[2]	0	R/W	Audio Engine Reset 0 = Normal 1 = Reset Audio Registers & Wave Engine State Machines When this bit is '1', the audio block (including wavetable and legacy audio) will be reset. It must be set to '0', to exit reset.
[1]	0	R/W	Sub-System Vendor ID Write Enable 0 = Sub-System Vendor ID is Read Only 1 = Sub-System Vendor ID is Read/Write
[0]	0	R	Reserved

4.1.3 Power Management Configuration

4.1.3.1 Capabilities ID (Offset = 48h)

Bits	POR	Read/Write	Description
[7:0]	01h	R	Identifies the capability as being the PCI Power Management Registers.

4.1.3.2 Next Item Pointer (Offset = 49h)

Bits	POR	Read/Write	Description
[7:0]	00h	R	By being 00h, indicates the end of the linked-list of extended capabilities.

4.1.3.3 Power Management Capabilities (Offset = 4Ah)

Bits	POR	Read/Write	Description
[15:11]	00000b	R	PME Support – The 4DWAVE-DX does not support PME# generation.
[10]	1	R	D2 Support – The 4DWAVE-DX supports D2 power state.
[9]	1	R	D1 Support – The 4DWAVE-DX supports D1 power state.
[8:6]	000b	R	Reserved
[5]	0	R	Device Specific Initialization – The 4DWAVE-DX does not require any device specific initialization.
[4]	0	R	Auxiliary Power Source – The 4DWAVE-DX does not support separate internal power support. (Or PME# generation.)
[3]	0	R	PME Clock - The 4DWAVE-DX does not support PME# generation and, therefore, does not need the PCI clock to generate a PME#.
[2:0]	001b	R	Version – The 4DWAVE-DX support Revision 1.0 of the PCI Power Management Interface specification.

4.1.3.4 Power Management Control/Status (Offset = 4Ch)

Bits	POR	Read/Write	Description
[15]	0	R	PME Status – The 4DWAVE-DX does not support PME generation.
[14:13]	00b	R	Data Scale – The 4DWAVE-DX does not support Power value reporting through the "Data" register.
[12:9]	0000b	R	Data Select – The 4DWAVE-DX does not support Power value reporting through the "Data" register.
[8]	0	R	PME# Enable – The 4DWAVE-DX does not support PME# generation.
[7:2]	000000b	R	Reserved
[1:0]	00b	R/W	Power State – This is used to determine the current power state. Software updates this register when changing power states 00b – D0 01b – D1 10b – D2 11b-D3hot

4.1.4 Interrupt Snooping Configuration

4.1.4.1 Interrupt Snooping Control (Offset = 50h)

Bits	POR	Read/Write	Description
[15:8]	00h	R/W	Interrupt Vector: Compared to vector returned on AD[7:0] during a PCI interrupt acknowledge cycle. If it matches, then disable INTA# until all internal interrupts have been cleared.
[7:1]	00h	R	Reserved
[0]	0	R/W	Interrupt Snoop Enable 0 = Disable Interrupt Snooping 1 = Enable Interrupt Snooping (During Interrupt Acknowledge)

4.2 Wave Engine and Control Registers

4.2.1 Address Map and Wave Register Space

The 4DWAVE-DX can be configured to respond to the separate legacy register addresses (SoundBlaster™, Adlib, MPU401, and Game Port), as well as the combined Wave register space (AudioBase). The Wave register space can be accessed through traditional I/O cycle or memory mapped I/O cycles, but the legacy register space is only accessible through I/O cycles. The Legacy registers are mapped into the bottom 64 bytes of the Wave register address space. Figure 4-1 below shows the System I/O and Memory address space for 4DWAVE-DX.

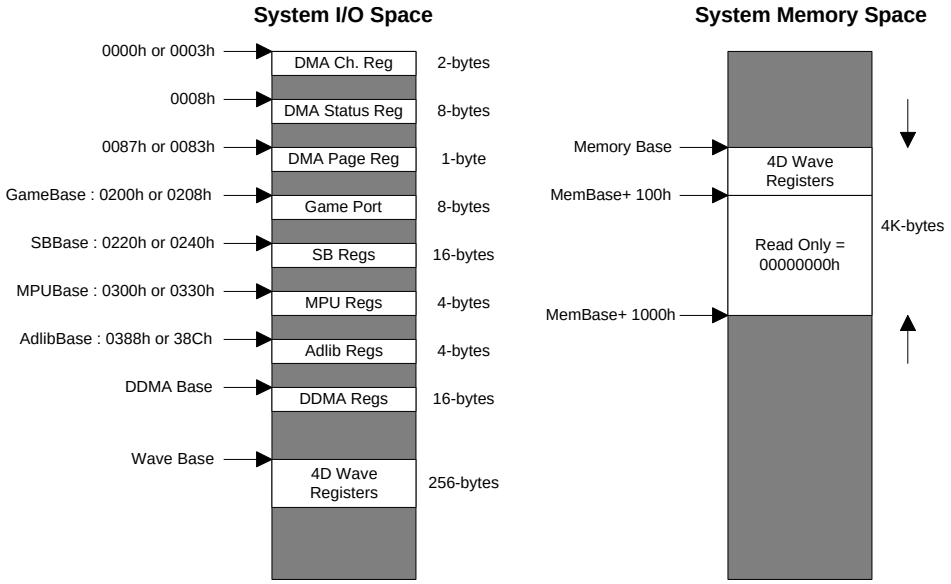


Figure 4-1. System I/O and Memory Address Space of 4DWAVE-DX

Table 4.2 details the address map of the 4DWAVE-DX internal register set. These Wave registers are addressable using either the Audio I/O Base Address or the Audio Memory Base Address. The legacy portion of these registers is available through their respective legacy addresses as well. By providing both an I/O and a memory aperture to these registers, the 4DWAVE-DX can be tuned for both compatibility and performance. Both I/O and Memory apertures can be enabled simultaneously.

The Wave registers consume a 256-byte aligned address space. The I/O mapping only allows the 256-byte space to be accessed. The memory mapping consumes 4K-bytes, however, only the bottom 256-bytes actually addresses the Wave registers. All register contents reside on-chip, however, some registers must be accessed through a base indexed manner. This is true for voice channel specific registers and OPL3 RAM locations. All I/O locations which are not defined will return H'00000000 when read. There is no affect when writing to undefined registers.

The Wave registers indexed by 00h through DFh are global in function and are not specific to a particular voice channel.

The registers E0h through EFh are voice channel specific for each of the 64 voice channels (0-63) and the channel index is programmed through CIR (Channel Index Register) at offset A0h. Registers F0h through FFh are implemented only for the first 32 voice channels.

Table 4-2. 4DWAVE-DX Internal Registers

Audio Base Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
00	DMAR3	DMAR2	DMAR1	DMAR0
04	RSVD	DMAR6	DMAR5	DMAR4
08	DMAR11	DMAR10	RSVD	DMAR8
0C	DMAR15	DMAR14	DMAR13	DMAR12
10	SBR3/SBR1	SBR2	SBR1/SBR3	SBR0
14	SBR6	SBR6	SBR5	SBR4
18	SBR7	SBR7	RSVD	RSVD
1C	SBR10	SBR9	SBR8	SBR8
20	MPUR3	MPUR2	MPUR1	MPUR0
24-2C	RSVD (Read Only = h'00000000)			
30	RSVD	RSVD	GAMER1	GAMER0
34	GAMER2			
38	GAMER3			
3C	RSVD (Read Only = h'00000000)			
40	ACR0			
44	ACR1			
48	ACR2			
4C	RSVD (Read Only = h'00000000)			
50	ASR0			
54	RSVD	ASR2	ASR1	
58	ASR3			
5C	ASR6	ASR5	RSVD	ASR4
60	AOPLSR0			
64-6C	RSVD (Read Only = h'00000000)			
70	RSVD	RCI2	RCI1	RCI0
74	RSVD (Read Only = h'00000000)			
78	PSBVLD_A Channels 0-31			
7C	PSBVLD_B Channels 32-63			
80	START_A Channels 0-31			
84	STOP_A Channels 0-31			
88	DLY_A			
8C	SIGN_CSO_A			
90	CSPF_A Channels 0-31			
94	CEBC_A			
98	AIN_A Channels 0-31			
9C	EINT_A			

Table 4-2. 4DWAVE-DX Internal Registers (Cont'd.)

Audio Base Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
A0	GC(12:8) +LFOCTRL_A	LFOCOUNT_A	GC(7:0)	CIR (Channel Index Register)
A4	AINTEN_A Channels 0-31			
A8	MUSICVOL		WAVEVOL	
AC	SBDELTA		DELTA_R	
B0	MISCINT			
B4	START_B Channels 32-63			
B8	STOP_B Channels 32-63			
BC	CSPF _B Channels 32-63			
C0	SBBL		SBCL	
C4	SBE2R	RSVD	SBDD	SBCTRL
C8	RSVD	STIMER		
CC	LFOCTRL_B	LFOCOUNT_B	ROM_TEST	
D0	T_FIFO [FIFO(39:24)]		T_FIFO [FIFO(19:4)]	
D4	T_DIGIMIXER [ADL(19:4)]		T_DIGIMIXER [ADR(19:4)]	
D8	AIN_B Channels 32-63			
DC	AINTEN_B Channels 32-63			
Bank A Address RAM (Channels 0-31)				
E0	CSO		ALPHA(11:4)	ALPHA(3:0) + FMS
E4	PSBPTR[1:0] + LBA[29:0]			
E8	ESO		DELTA	
EC	RSVD	RSVD	FMC + RVOL(6:1)	RVOL(0) + CVOL
Bank B Address RAM (Channel 32-63)				
E0	CSO		ALPHA(11:4)	ALPHA(3:0) + FMS
E4	PSBPTR[1:0] + LBA[29:0]			
E8	ESO		DELTA	
EC	RSVD	RSVD	FMC + RVOL(6:1)	RVOL(0) + CVOL
Bank A Envelope RAM				
F0	GVSEL + PAN	VOL	CTRL + Ec(11:8)	Ec(7:0)
F4	EBUF1			
F8	EBUF2			
FC	RSVD (Read Only = h'00000000)			

4.2.2 Legacy Registers I/O Mapping and Wave Engine Registers

4.2.2.1 Legacy Registers I/O Address and Wave Register Space I/O Mapping

AudioBase Offset	Register Name	Legacy I/O Address	Bits	POR	R/W	Description
Legacy DMA Channel Mapping Registers						
00h	DMAR0	0000h/0002h	[7:0]	00h	R/W	Legacy DMA Playback Buffer Base Register 1
01h	DMAR1	0000h/0002h	[7:0]	00h	R/W	Legacy DMA Playback Buffer Base Register 2
02h	DMAR2	0087h/0083h	[7:0]	00h	R/W	Legacy DMA Playback Buffer Base Register 3
03h	DMAR3	--	[7:0]	00h	R/W	Legacy DMA Playback Buffer Base Register 4
04h	DMAR4	0001h/0003h	[7:0]	00h	R/W	Legacy DMA Playback Byte Count Register 1
05h	DMAR5	0001h/0003h	[7:0]	00h	R/W	Legacy DMA Playback Byte Count Register 2
06h	DMAR6	--	[7:0]	00h	R/W	Legacy DMA Playback Byte Count Register 3
08h	DMAR8	0008h	[7:0]	00h	R	Legacy DMA Command/Status Register
0Ah	DMAR10	000Ah	[7:0]	00h	W	Legacy DMA Single Channel Mask Port
0Bh	DMAR11	000Bh	[7:0]	00h	W	Legacy DMA Channel Operation Mode Register
0Ch	DMAR12	000Ch	[7:0]	00h	W	Legacy DMA First/Last Flag Clear Port
0Dh	DMAR13	000Dh	[7:0]	00h	W	Legacy DMA Master Clear Port
0Eh	DMAR14	000Eh	[7:0]	00h	W	Legacy DMA Clear Mask Port
0Fh	DMAR15	000Fh	[7:0]	0bh	W	Legacy DMA Multi-Channel Mask Register
Legacy SB Mapping Registers						
10h	SBR0	SBBase+0h	[7:0]	00h	R/W	Legacy FM Music Bank 0 Register Index/Legacy FM Music Status
11h	SBR1/SBR3	SBBase+1h/ SBBase+3h	[7:0]	00h	R/W	Legacy FM Music Bank 0/1 Register Data Port
12h	SBR2	SBBase+2h	[7:0]	00h	R/W	Legacy FM Music Bank 1 Register Index
13h	SBR3/SBR1	SBBase+1h/ SBBase+3h	[7:0]	00h	R/W	Legacy FM Music Bank 0/1 Register Data Port
14h	SBR4	SBBase+4h	[7:0]	00h	R/W	Legacy SB Mixer Register Index Port
15h	SBR5	SBBase+5h	[7:0]	XXh	R/W	Legacy SB Mixer Register Data Port
16-17h	SBR6	SBBase+6h/ SBBase+7h	[7:0]	FFh	W (R=FFh)	Legacy SB ESP Reset Port
1A-1Bh	SBR7	SBBase+Ah/+Bh	[7:0]	AAh	R	Legacy SB ESP Data Port
1C-1Dh	SBR8	SBBase+Ch/+Dh	[7:0]	00h	R/W	Legacy SB Command/Status Port
1Eh	SBR9	SBBase+Eh	[7:0]	2Ah	R	Legacy SB ESP Data Ready/IRQ Ack Port 1

(Continued on the next page)

AudioBase Offset	Register Name	Legacy I/O Address	Bits	POR	R/W	Description
Legacy SB Mapping Registers						
1Fh	SBR10	SBBase+Fh	[7:0]	2Ah	**R**	Legacy SB ESP Data Ready/IRQ Ack Port 2
Legacy MPU-401 Mapping Registers						
20h	MPUR0	MPU401Base+0h	[7:0]	XXh	R/W	Legacy MPU-401 Data Port/IRQ Ack Port
21h	MPUR1	MPU401Base+1h	[7:0]	80h	R/W	Legacy MPU-401 Command/ Status Port
22h	MPUR2	MPU401Base+2h	[7:0]	10h	[7:2] R/W [1:0] R	MPU-401 Operation Control/ Status Register
23h	MPUR3	MPU401Base+3h	[7:0]	XXh	R	MPU-401 MIDI-IN FIFO Access Port
Legacy Game Port Mapping and Digital Enhanced Game Port Registers						
30h	GAMER0	--	[7:0]	00h	R/W	Game Port Control Register
31h	GAMER1	GameBase + 0h - 7h	[7:0]	F0h	R/W	Legacy Game Port I/O Register
34h	GAMER2	--	[31:0]	FFFFFFFFh	R/W	Enhanced Game Port Position Register 1
38h	GAMER3	--	[31:0]	FFFFFFFFh	R/W	Enhanced Game Port Position Register 2

4.2.2.2 Wave Engine Registers

AudioBase Offset	Register Name	Bits	POR	R/W	Description
AC '97 Control Registers					
40h	ACR0	[31:0]	00000000h	R/W	AC '97 Codec Write Register
44h	ACR1	[31:0]	00000000h	R/W	AC '97 Codec Read Register
48h	ACR2	[31:0]	00000000h	R/W	AC '97 Command/Status Register
Miscellaneous Status/Control Registers					
50h	ASR0	[31:0]	00000000h	R	4DWAVE-DX Status Register
54h	ASR1	[15:0]	AC44h	R	Legacy SB Frequency Readback Register
56h	ASR2	[7:0]	F5h	R	Legacy SB Time Constant Readback Register
58h	ASR3	[31:0]	00000000h	R/W	4DWAVE-DX Scratch-pad Register
5Ch	ASR4	[7:0]	01h	R	4DWAVE-DX Version Control Register
5Eh	ASR5	[7:0]	04h	R/W	SB ESP Version High Byte Control Register
5Fh	ASR6	[7:0]	02h	R/W	SB ESP Version Low Byte Control Register
OPL3 Channel Status Registers					
60h	AOPLSR0	[31:0]	00000000h	R	OPL3 Emulation Channel Key On/Off Trace Register
Recording Channel/Streaming Buffer Status Registers					
70h	RCI[2:0]	[31:0]	00000000h	R	Record Channel Index 2 (Chorus), 1 (Reverb), 0 (Mixer) Register
78h	PSBVLD_A	[31:0]	00000000h	R/W	Bank A PCI Stream Buffer Valid Flags (for testing only)
7Ch	PSBVLD_B	[31:0]	00000000h	R/W	Bank B PCI Stream Buffer Valid Flags (for testing only)

(Continued on the next page)

AudioBase Offset	Register Name	Bits	POR	R/W	Description
4DWAVE-DX Wave Engine Registers					
80h	START_A	[31:0]	00000000h	R/W	Bank A START Command and Status Register
84h	STOP_A	[31:0]	00000000h	R/W	Bank A STOP Command and Status Register
88h	DLY_A	[31:0]	00000000h	R/W	Delay Flag Register (Bank A only)
8Ch	SIGN_CSO_A	[31:0]	00000000h	R/W	Sign Bit of CSO (Bank A only)
90h	CSPF_A	[31:0]	00000000h	R	Bank A Current Sample Position Flag
94h	CEBC_A	[31:0]	00000000h	R/W	Current Envelope Buffer Control Register (Bank A only)
98h	AIN_A	[31:0]	00000000h	R/W	Bank A Address Engine Interrupt Register
9Ch	EINT_A	[31:0]	00000000h	R/W	Envelope Engine Interrupt Register (Bank A only)
A0h	LFO_A	[31:0]	00000000h	R/W	Bank A LFO, Global Control and Channel Index Register
A4h	AINTEN_A	[31:0]	00000000h	R/W	Bank A Address Engine Interrupt Enable Control Register
A8h	VOL_A	[31:0]	00008080h	R/W	Global Music Volume and Global Wave Volume Control Register
ACh	DELTA	[31:0]	00000000h	R/W	Sample Change Step for Legacy SB Voice In/Out & Recording
B0h	MISCINT	[31:0]	00000000h	R/W	Record/Playback Underrun/Record Overrun Interrupt Register
B4h	START_B	[31:0]	00000000h	R/W	Bank B START Command and Status Register
B8h	STOP_B	[31:0]	00000000h	R/W	Bank B STOP Command and Status Register
BCh	CSPF_B	[31:0]	00000000h	R	Bank B Current Sample Position Flag
C0h	SBBL&SBCL	[31:0]	00000000h	R/W	SB DMA Base Length & SB DMA Current Length Register
C4h	SBCTRL	[31:0]	00000000h	R/W	SB Control/SB DMA Testing Byte/SB Direct Playback Data
C8h	STIMER	[31:0]	00000000h	R	Sample Timer
CCh	ROM_TEST	[15:0]	XXXXh	R	ROM Test Register
CEh	LFO_B	[15:0]	0000h	R/W	Bank B LFO Register
D0h	T_FIFO	[31:0]	XXXXXXXXh	R	Mixer FIFO Test Register
D4h	T_DIGIMIXER	[31:0]	XXXXXXXXh	R	Mixer Accumulator Test Register
D8h	AIN_B	[31:0]	00000000h	R/W	Bank B Address Engine Interrupt Register
DCh	AINTEN_B	[31:0]	00000000h	R/W	Bank B Address Engine Interrupt Enable Control Register

4.2.2.3 Channel-Specific Registers

There are 64 independent voice channels. The first 32 voice channels are designated Bank A. The second 32 voice channels are designated Bank B. Every voice channel has it's own parameter register set. Bank A and Bank B parameters differs slightly. These 64 register sets will share the same I/O space (offset E0h – EFh). The global register CIR (offset A0h) is used to select the current accessible channel.

AudioBase Offset	Register Name	Bits	POR	R/W	Description
E0h	CSO & Alpha & FMS	[31:0]	XXXXXXXXh	R/W	Current Sample Offset & Sample Interpolation Coefficient & Frequency Modulation Step
E4h	PPTR & LBA	[31:0]	XXXXXXXXh	R/W	PSB Pointer & Loop Begin Address
E8h	ESO & DELTA	[31:0]	XXXXXXXXh	R/W	End Sample Offset & Delta Sample Rate Ratio
ECh	FMC & RVOL & CVOL	[31:0]	XXXXXXXXh	R/W	FM Control, Reverb Volume & Chorus Volume Control

4.2.2.4 Global Volume Control and Bank A Envelope Control Registers

AudioBase Offset	Register Name	Bits	POR	R/W	Description
F0h	GVSEL & MISC	[31:0]	XXXXXXXXh	R/W	Global Volume Select, PAN & Volume Attenuation, Control and Current Envelope
F4h	EBUF1	[31:0]	XXXXXXXXh	R/W	Envelope Buffer 1
F8h	EBUF2	[31:0]	XXXXXXXXh	R/W	Envelope Buffer 2

4.3 Legacy Compatibility

The 4DWAVE-DX supports all aspects of SoundBlaster™ legacy compatibility. Including OS Compatibility, I/O Address, Compatibility, Legacy Functions Compatibility (including, OPL3, SoundBlaster™ Pro/16 Mixer, MPU-401, Game Port) which includes ISA DMA and IRQ compatibility. The following sections will briefly describe how each compatibility is achieved.

4.3.1 OS Compatibility

The 4DWAVE-DX supports all major OSs. Each OS environment involves different levels and types of compatibility. The type of compatibility and the mechanism to attain it are covered in the table below.

Application OS	Compatibility Type
Real-mode DOS	Hardware register and function compatibility of SoundBlaster™ 16, Adlib, OPL3, MIDI, Game Port and ISA DMA
Windows® 3.1/95 DOS-Box	Hardware register and function compatibility of SoundBlaster™ 16, Adlib, OPL3, MIDI, Game Port and ISA DMA
Windows® 98 DOS-Box	Virtual register and function compatibility of SoundBlaster™ 16, Adlib, OPL3, MIDI, Game Port and ISA DMA

4.3.2 I/O Compatibility

The 4DWAVE-DX supports the legacy I/O spaces for the 8-bit 8237A (Master DMA Controller), the Adlib – OPL3, the MIDI MPU-401 UART, the SoundBlaster™ 16 (except the CD space), and the Game Port. These can be individually enabled and selected through the PCI Config registers.

Legacy Function	I/O Space	Enable Control	Address/Channel Select
8237A DMA Controller	0000h – 000Fh Channel 0 or 1	DMA Trapping Enable PCI Config [45h].bit1	Channel Select PCI Config [45h].bit0
Adlib	0388h – 038Bh or 038Ch – 038Fh	Address Decode Enable PCI Config [44h].bit3	Address Base Select PCI Config [44h].bit2
MIDI/ MPU-401 UART	0330h – 0333h or 0300h – 0303h	Address Decode Enable PCI Config [44h].bit7	Address Base Select PCI Config [44h].bit6
SoundBlaster™ 16	0220h – 022Fh or 0240h – 024Fh	Address Decode Enable PCI Config [44h].bit1	Address Base Select PCI Config [44h].bit0
Game Port	0200h – 0207h or 0208h – 020Fh	Address Decode Enable PCI Config [44h].bit5	Address Base Select PCI Config [44h].bit4

4.3.3 Legacy Functions Compatibility

4DWAVE-DX provides legacy compatibility with SoundBlaster™ Pro/16 OPL3, Mixer, MPU-401 UART and Game Port as well as ISA DMA and IRQ compatibility. Legacy Audio can be configured through the PCI Configuration registers. These registers include setting and control for Distributed DMA and Trident proprietary DMA emulation mechanism.

4.3.3.1 SoundBlaster™ Pro/16 OPL3

The 4DWAVE-DX uses a proprietary VirtualFM™ technology to perform the emulation of the OPL3 function through a combination of hardware and software. The complete OPL3 register set is implemented and VirtualFM™ driver uses several additional status and control register to assist in OPL3 emulation. Some of the registers are implemented with the complete function as in the OPL3. Other registers just hold the data for the VirtualFM™ driver to act on. The 4DWAVE-DX has added an AOPLSR0 register. This register is used to hold the status of which OPL3 keys, music or rhythm, have been turned off or on. This register automatically clears itself once it is read.

4.3.3.2 SoundBlaster™ Pro/16 Mixer

The SoundBlaster™ Pro/16 Mixer is used to control the various volume levels. The 4DWAVE-DX uses the CT1745 mixer register set. The complete SoundBlaster™ 16 and SoundBlaster™ Pro mixer register sets are implemented. All mixer registers are implemented in

hardware. The 4DWAVE-DX performs the emulation of the mixer function through a combination of hardware and software. The driver will convert the command and program the AC '97 mixer register accordingly.

4.3.3.3 MIDI & MPU-401 UART

There are two ways to use MIDI in SoundBlaster™-compatible implementation. (1) MPU-401 UART and (2) MIDI Synthesizer. Applications using the MPU-401 UART mode send/receive the MIDI command/data through the UART with a standard 2-pin interface (MIDI-IN and MIDI-OUT). The protocol is based on 8 bits of data with 1-start and 1-stop bit. This mode is used for user connecting the external keyboard or organ with MIDI IN/OUT capability for playback and record. The MIDI Synthesizer mode also uses the MPU-401 UART, however, rather than transferring the MIDI data through the UART. The data is captured and processed by the VirtualGM™/VirtualGS™ driver. The driver interprets the MIDI command/data and converts its corresponding instruments or wavetable sample for playback.

4.3.3.4 Game Port

The Digital Enhanced Game Port in 4DWAVE-DX is completely backward compatible with the legacy game port 8-bit register. In legacy compatibility mode (either DOS or Windows® without DirectInput™ driver loaded), it works with any joysticks intended for the legacy game port. With the DirectInput™ driver loaded, the Digital Enhanced Game Port will substantially enhance system and gaming performance by eliminating most of the I/O polling overhead (up to 12% CPU).

4.3.3.5 SoundBlaster™ DMA

The SoundBlaster™ uses an 8-bit DMA channel. In typical system configuration, DMA channels 0, 1 are available. The SoundBlaster™ will default to channel 1. On 4DWAVE-DX, channel 0 or 1 can be selected. 4DWAVE-DX supports two legacy DMA compatibility mechanisms : (1) The first type is based on the industry Distributed DMA (DDMA Rev. 6.0) standard which requires the system chipset to contain DDMA Master logic, and (2) the second type of legacy requires no DDMA support by the system chipset but is also founded on the DDMA concept. With a "fair arbiter" design in all the system core logic, both mechanisms assume that when the legacy DMA cycle is "retried" on PCI, that a different PCI Master will be allocated the PCI Bus and not the PCI Master issuing the legacy DMA cycle.

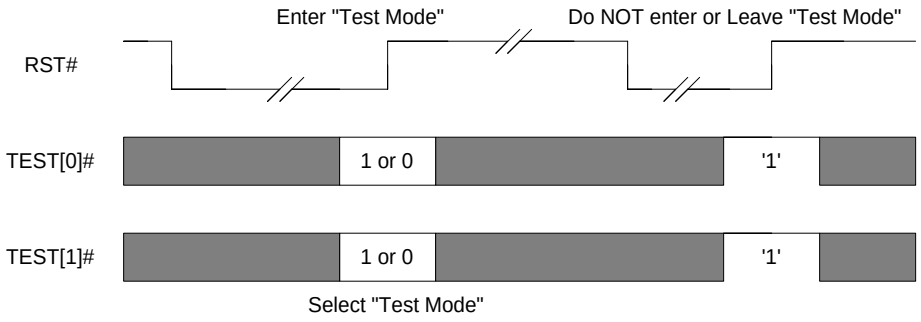
Distributed DMA is an industry standard mechanism for supporting legacy DMA cycles on a PCI Bus. It requires a DDMA-compliant system chipset to support the DDMA Master function (responsible for redirecting and gathering control bits from trapped legacy DMA cycles). 4DWAVE-DX implements the corresponding logic to support a DDMA Slave function (responsible for sending and receiving DMA control information with the DDMA Master). If the system chipset does not support DDMA, the 4DWAVE-DX will use Mechanism (2) above to provide both the "slave" and "master" functionality which is specifically limited to the audio sub-system.

5 System Test Functions

The 4DWAVE-DX has two test modes to assist in board debugging and trouble-shooting during manufacturing. The two test modes are “Global Tristate” and “XOR tree.”

5.1 Test Mode

The 4DWAVE-DX uses the TEST[1:0]# pins in conjunction with the RST# pin to enter “test mode”. When RST# transitions from a low (active) to an high (inactive), if TEST[1:0]# are both not a logical ‘1’ (high), the device enters a test mode.



The device uses the TEST[1:0]# pins to determine which test mode is selected.

Test Mode	TEST[1]#	TEST[0]#
Normal	**1**	**1**
XOR Tree	**1**	**0**
Global Tristate	**0**	**1**
Reserved	**0**	**0**

To leave Test Mode, the device must be reset with both the TEST[1:0]# pins as a logical ‘1’. Both TEST[1:0]# pins have an internal Pull-Up in the pad.

5.2 Global Tristate

The Global Tristate test mode will put all outputs into a high impedance state so that no pin is driving a trace. This allows system designers to check board trace connectivity or inject input test patterns to other on-board devices (such as AC ’97) without interference from the 4DWAVE-DX.

5.3 XOR Tree

The XOR tree test mode will put all signals into an input mode with a single pin, TDO, as an output. The inputs are chained together into a single XOR tree. This test mode is used to determine if all pads have been correctly attached to the board. When toggling any of the input pins, the output pin will also toggle.

TDO (Pin 70) is used as the XOR tree output. The RST# and TEST[1:0]# pins are not connected to the XOR tree. All other signals are inputs in this test mode.

6 AC/DC Parameters

6.1 DC Parameters

Tambient = 25C

Vcc=5.0V +/- 5% or 3.3V +/- 10%

CVcc= 3.3V +/- 5%

Vss = CVss = 0V

6.1.1 Core (3.3V Only)

Symbol	Parameter	Condition	Min	Max	Units	Notes
CVcc	Core Supply Voltage		3.15	3.45	V	
CVss	Core Ground		0	0	V	

6.1.2 I/O – 5V Signaling Environment

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vcc	I/O Supply Voltage		4.75	5.25	V	
Vss	I/O Ground		0	0	V	
Vih	Input High Voltage		2.0		V	1
Vil	Input Low Voltage			0.8	V	1
Voh	Output High Voltage		2.4		V	1
Vol	Output Low Voltage			0.55	V	1

Note: Consistent with both AC '97 Rev 1.13 and PCI 2.1 specifications.

6.1.3 I/O – 3.3V Signaling Environment

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vcc	I/O Supply Voltage		3.0	3.6	V	
Vss	I/O Ground		0	0	V	
Vih	Input High Voltage		1.5		V	1
Vil	Input Low Voltage			1.0	V	1
Voh	Output High Voltage		2.97		V	1
Vol	Output Low Voltage			0.33	V	1

Note : Consistent with both AC '97 Rev 1.13 and PCI 2.1 specifications.

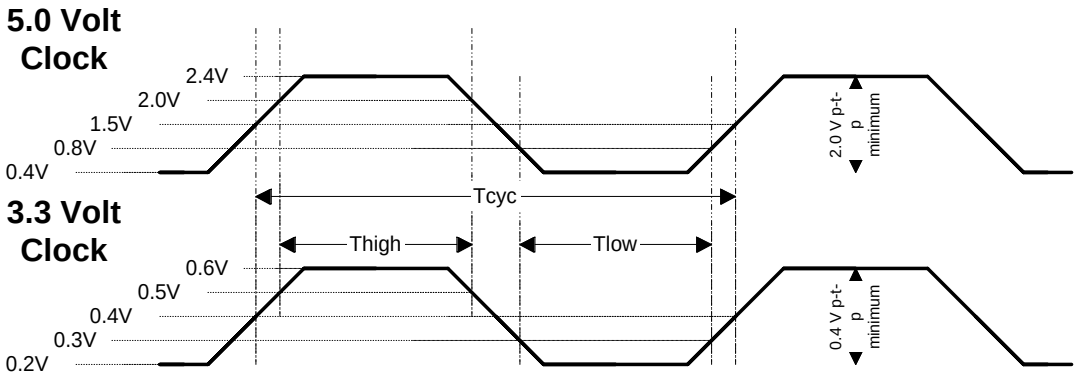
6.2 AC Parameters

6.2.1 Clocks

6.2.1.1 PCI Clock

Symbol	Parameter	Condition	Min	Max	Units	Notes
Tcyc	CLK Cycle Time		30		ns	1
Thigh	CLK High Time		11		ns	
Tlow	CLK Low Time		11		ns	
Tskew	CLK Skew			2	ns	

Note : 1) In general, all PCI components must work with any clock frequency between DC and 33MHz.



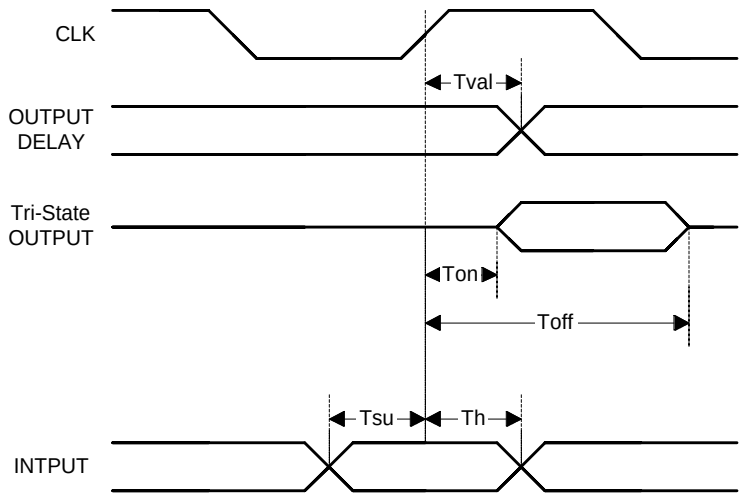
6.2.2 PCI Signals

PCI Inputs: AD[31:0], C_BE_N[3:0], FRAME_N, IRDY_N, TRDY_N, STOP_N, DEVSEL_N, IDSEL, PAR, GNT_N

PCI Outputs: AD[31:0], C_BE_N[3:0], FRAME_N, IRDY_N, TRDY_N, STOP_N, DEVSEL_N, PAR, REQ_N, INTA_N, PERR_N, SERR_N

Point-to-Point Signals: REQ_N, GNT_N

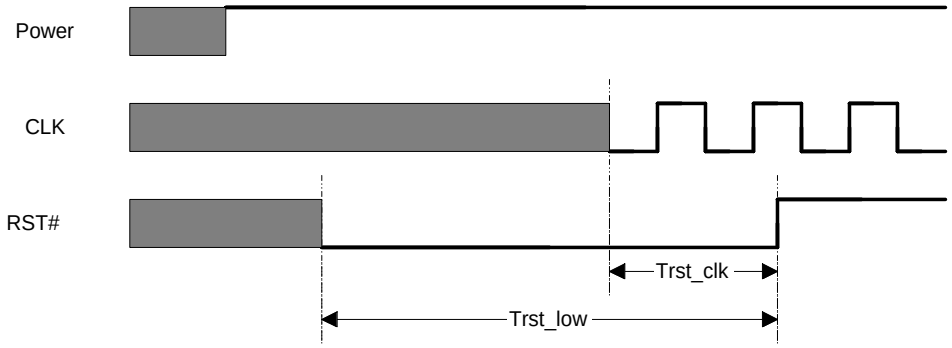
Symbol	Parameter	Condition	Min	Max	Units	Notes
Tval_bus	CLK to PCI Output Valid Delay – bussed signals		2	11	ns	
Tval_ptp	CLK to PCI Output Valid Delay – point to point signals		2	12	ns	
Ton	PCI Output float to active		2		ns	
Toff	PCI Output active to float			28	ns	
Tsu_bus	PCI Input set up time to CLK – bussed signals		7		ns	
Tsu_gnt	PCI Input set up time to CLK – GNT_N		10		ns	
Tsu_gnt	PCI Input set up time to CLK – REQ_N		12		ns	
Th	PCI Input hold time from CLK		1.5		ns	



6.2.3 Resets

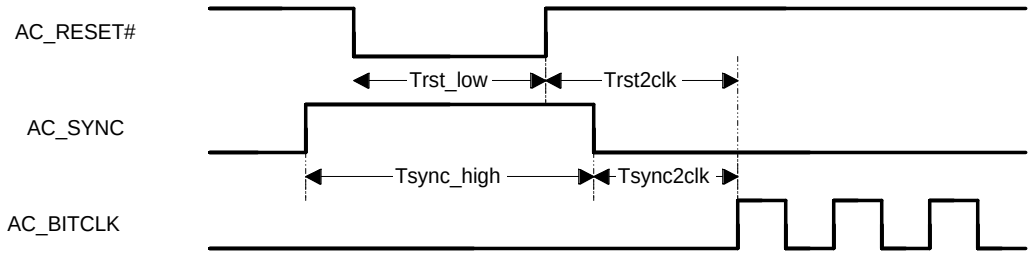
6.2.3.1 PCI Reset

Symbol	Parameter	Condition	Min	Max	Units	Notes
Trst_low	RST# low time after power stable		1		ms	
Trst_clk	RST# low time after CLK stable		100		us	



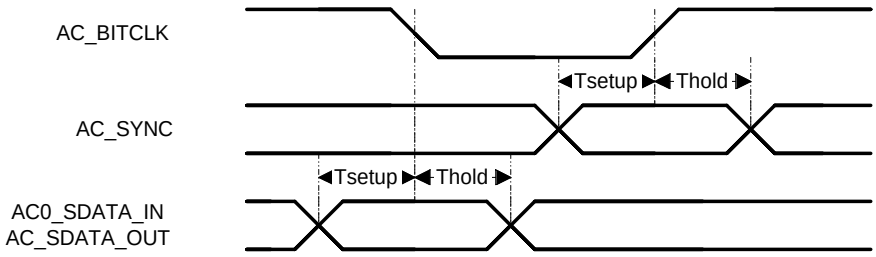
6.2.3 AC '97 Reset (Cold and Warm)

Symbol	Parameter	Condition	Min	Max	Units	Notes
Trst_low	AC_RESET# low time		1		us	SW controlled or linked to PCIRST#
Trst2clk	AC_RESET# inactive to AC_BITCLK starts		200		ns	
Tsync_high	AC_SYNC high time		1.3		us	SW controlled
Tsync2clk	AC_SYNC inactive to AC_BITCLK starts		200		ns	

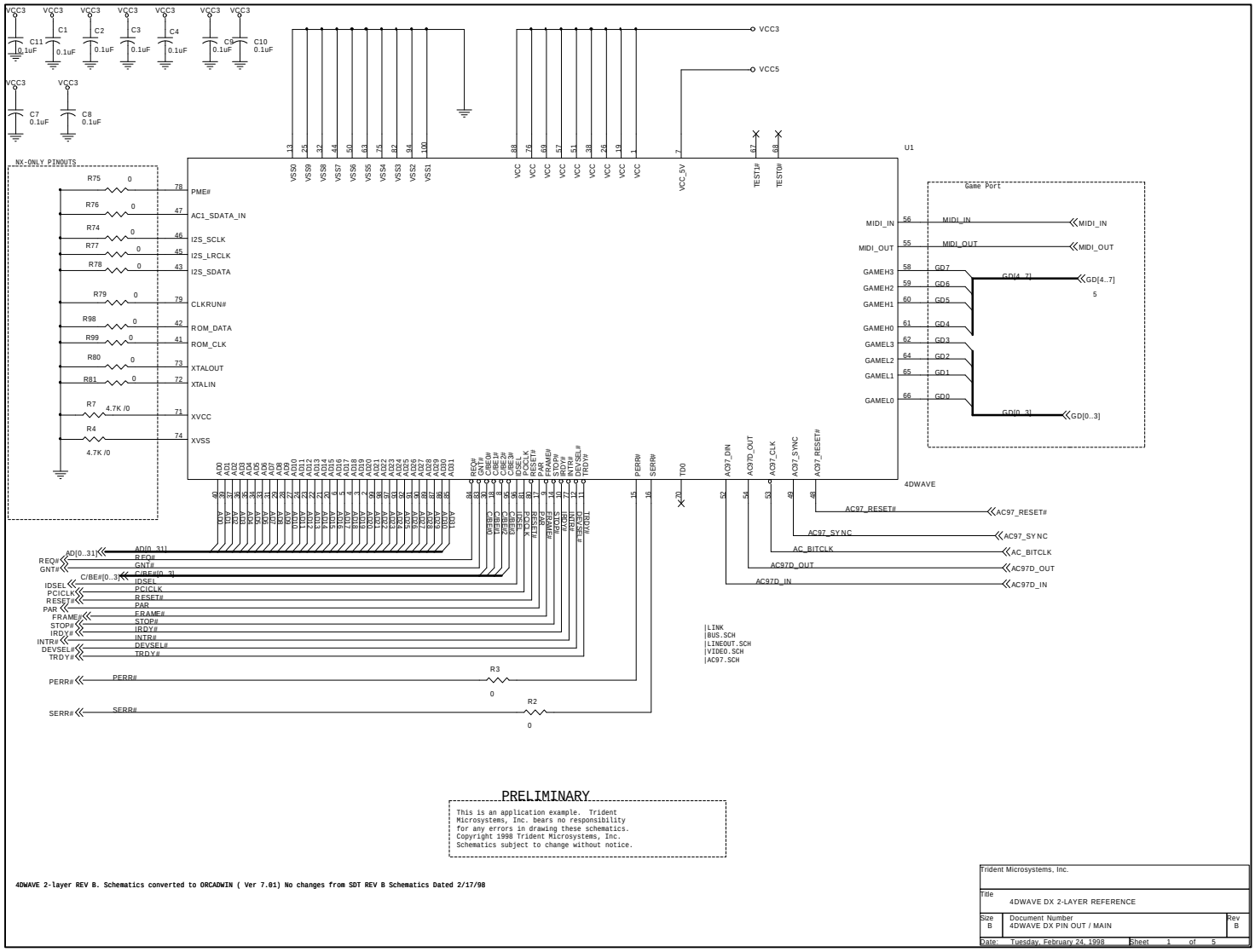


6.2.4 AC '97 Signals

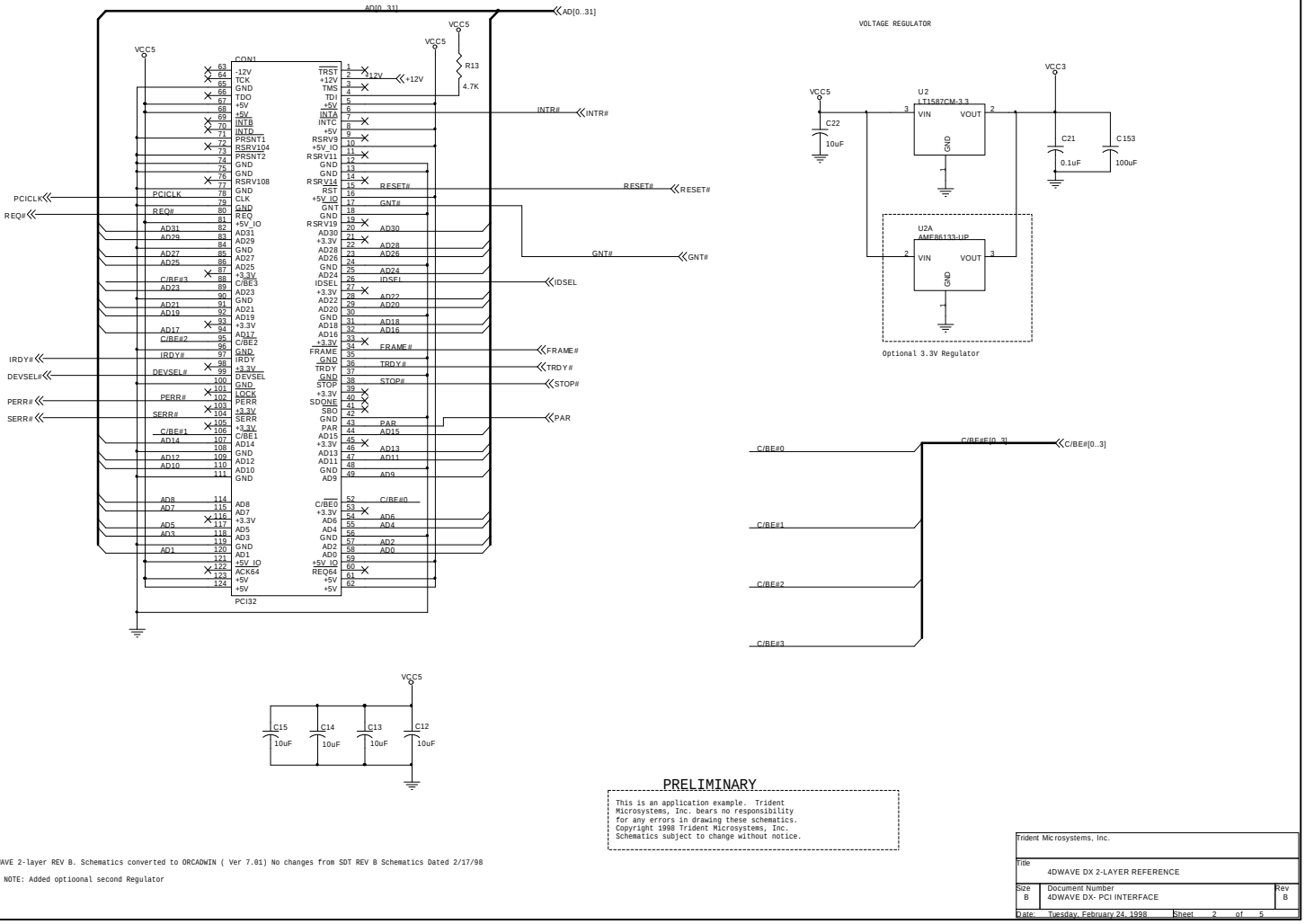
Symbol	Parameter	Condition	Min	Max	Units	Notes
Tsetup	Setup from edge of AC_BITCLK Falling Edge = AC0_SDATA_IN & AC_SDATA_OUT Rising Edge = AC_ SYNC		15		ns	
Thold	Hold from edge of AC0_BITCLK Falling Edge = AC0_SDATA_IN & AC_SDATA_OUT Rising Edge = AC_ SYNC		5		ns	



7 Reference Schematic



PCI LOCAL BUS

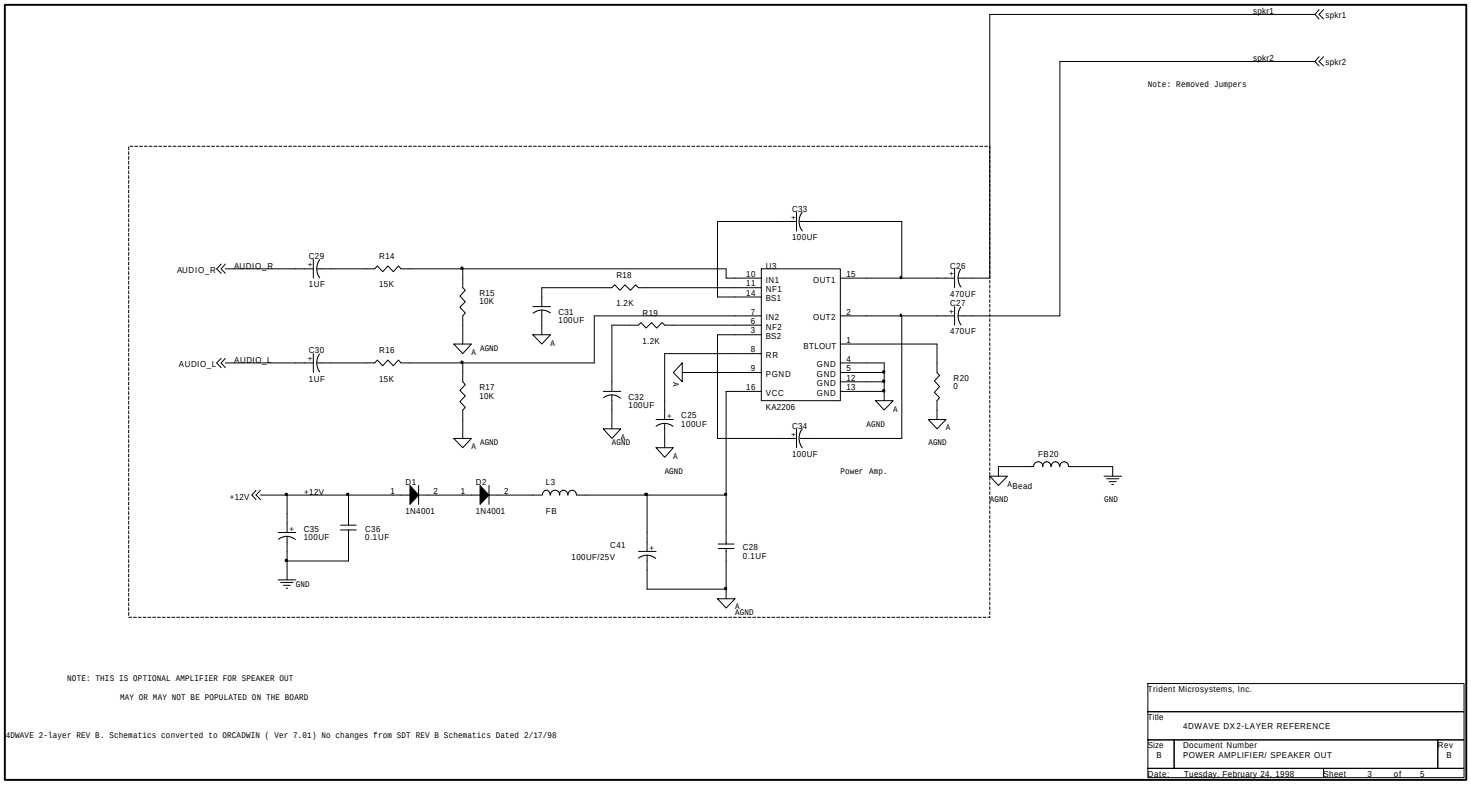


PRELIMINARY

4DWAVE 2-layer REV B. Schematics converted to ORCADWIN (Ver 7.01) No changes from SDT REV B Schematics Dated 2/17/98

NOTE: Added optioonal second Regulator

Trident Microsystems, Inc.		
Title: 4DWAVE DX 2-LAYER REFERENCE		
Size: B	Document Number: 4DWAVE DX- PCI INTERFACE	Rev: B
Date: Tuesday, February 24, 1998	Sheet 2 of 5	



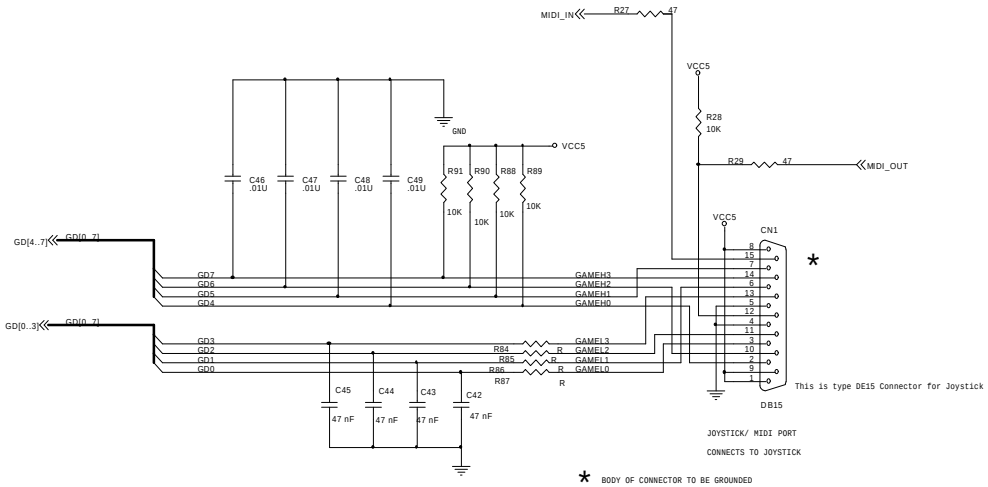
NOTE: THIS IS OPTIONAL AMPLIFIER FOR SPEAKER OUT

MAY OR MAY NOT BE POPULATED ON THE BOARD

4DWAVE 2-layer REV B. Schematics converted to ORCADWIN (Ver 7.01) No changes from SDT REV B Schematics Dated 2/17/98

Trident Microsystems, Inc.		
Title: 4DWAVE DX2-LAYER REFERENCE		
Size: B	Document Number: POWER AMPLIFIER/ SPEAKER OUT	Rev: B
Date: Tuesday, February 24, 1998	Sheet 3 of 5	

PRELIMINARY

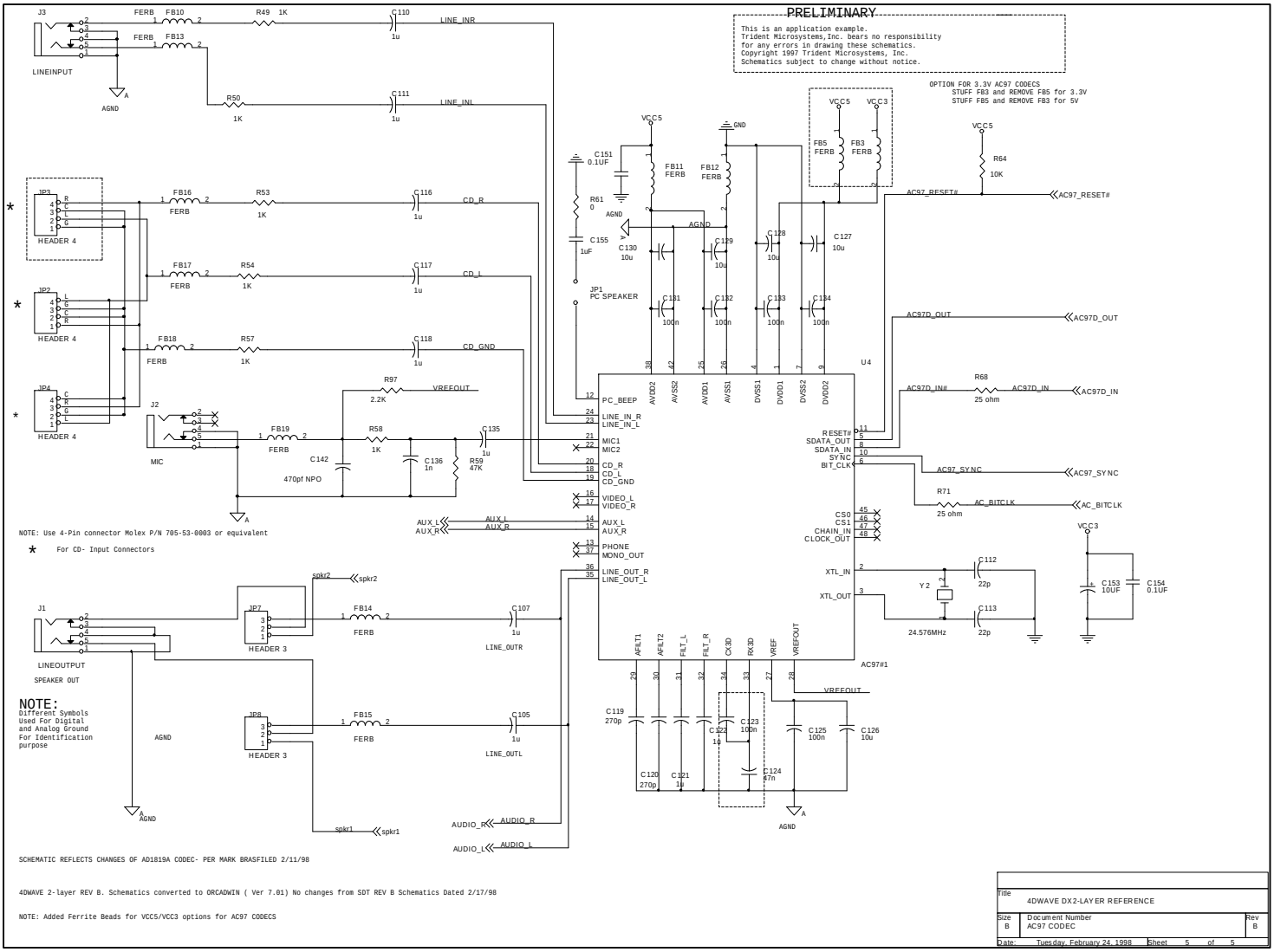


NOTE: R is 2.2K for R84,R85,R86,R87

NOTE: Reflects APG Recommendations

4DWAVE 2-layer REV B. Schematics converted to ORCADWIN (Ver 7.01) No changes from SDT REV B Schematics Dated 2/17/98

Trident Microsystems, Inc.		
Title: 4DWAVE DX 2-LAYER REFERENCE		
Size: B	Document Number: JOYSTICK /MIDI PORT ROM	Rev: B
Date: Tuesday, February 24, 1998	Sheet 4 of 5	


PRELIMINARY
This is an application example.
Trident Microsystems,Inc. bears no responsibility
for any errors in drawing these schematics.
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Schematics subject to change without notice.
OPTION FOR 3.3V AC97 CODECS
STUFF FB3 and REMOVE FB5 for 3.3V
STUFF FB5 and REMOVE FB3 for 5V
LINEINPUT
LINE_INR
LINE_INL
CD_R
CD_L
CD_GND
HEADER 4
MIC
470pf NPO
VREFOUT
AC97_RESET#
AC97D_OUT
AC97D_IN
AC97_SYNC
AC_BITCLK
25 ohm
PC_BEEP
LINE_IN_R
LINE_IN_L
MIC1
MIC2
VIDEO_L
VIDEO_R
AUX_L
AUX_R
PHONE
MONO_OUT
LINE_OUT_R
LINE_OUT_L
RESET#
SDATA_OUT
SDATA_IN
SYNC
BIT_CLK
CHAIN_IN
CLOCK_OUT
XTL_IN
XTL_OUT
24.576MHz
AC97#1
U4
JP1
PC SPEAKER
LINEOUTPUT
SPEAKER OUT
HEADER 3
LINE_OUTR
LINE_OUTL
AUDIO_R
AUDIO_L
AGND
NOTE:
Different Symbols
Used For Digital
and Analog Ground
For Identification
purpose
NOTE: Use 4-Pin connector Molex P/N 705-53-0003 or equivalent
* For CD- Input Connectors
SCHEMATIC REFLECTS CHANGES OF AD1819A CODEC- PER MARK BRASFILED 2/11/98
4DWAVE 2-layer REV B. Schematics converted to ORCADWIN (Ver 7.01) No changes from SDT REV B Schematics Dated 2/17/98
NOTE: Added Ferrite Beads for VCC5/VCC3 options for AC97 CODECS
Title
4DWAVE DX2-LAYER REFERENCE
Size B
Document Number AC97 CODEC
Rev B
Date: Tuesday, February 24, 1998
Sheet 5 of 5

8 4DWave-DX reference board Bill of Materials (Revised: April 23, 1998)

Item #	QTY	Reference	Part	Type/ Package	Comments/ Assembly
1	1	CN1	DB15	Joystick Connector	
2	1	CON1	PCI32	PCI Bus Edge Connector	
3a	12	C1,C2,C3,C4,C7,C8,C9,C10, C11,C21,C151,C154	0.1uF	Cap ceramic 50V SMD 0805	
3b	***2***	***C28,C36,***	***0.1uF***	***Cap ceramic 50V SMD 0805***	***Load For Amplifier. Default No LOAD***
4	6	C12,C13,C14,C15,C22, C153	10UF	Cap 25V Radial Thru-Hole	
5a	***6***	***C25,C31,C32,C33,C34, C35,***	***100UF***	***Cap 16V Radial Thru-Hole***	***Load For Amplifier. Default No LOAD***
5b	2	C41,C153	100UF	Cap 16V Radial Thru-Hole	
6	***12***	***C26,C27,***	***470uF***	***Cap 16V Can Thru-Hole***	***Load For Amplifier. Default No LOAD***
7	3	C29,C30,C105,C107, C110,C111,C116,C117, C118,C121,C122,C135, C155	1uF	Cap ceramic 50V SMD 0805	
8	8	C42,C43,C44,C45,C46,C47, C48,C49	.01uF	Cap ceramic 50V SMD 0805	
9	2	C113,C112	22pF	Cap ceramic 50V SMD 0805	
10	2	C119,C120	270pF	Cap ceramic 50V SMD 0805	

Item #	QTY	Reference	Part	Type/ Package	Comments/ Assembly
11	6	C123,C125,C131,C132, C133,C134	100nF	Cap ceramic 50V SMD 0805	
12	1	C124	47n	Cap ceramic 50V SMD 0805	
13	5	C126,C127,C128,C129, C130	10uF	Cap Radial Tantalum 16V Thru Hole	
14	1	C136	1n	Cap ceramic 50V SMD 0805	
15	1	C142	470pf NPO	Cap ceramic 50V SMD 0805	
16	***2***	***D1,D2***	***1N4001***	***Thru Hole axial***	***Load For Amplifier. Default No LOAD***
17a	2	FB3,FB5,[1]	FERB	Axial Ferrite Bead	Load One only. Default is FB5
17b	***11***	***FB10,FB11,FB12,FB13, FB14,FB15,FB16,FB17, FB18,FB19,FB20***	***FERB***	***Axial Ferrite Bead***	***Load For Amplifier. Default No LOAD***
18	1	JP1	PC SPEAKER Header	1X2 Header	
19	3	JP2,JP3,JP4	HEADER 4	1X4 Header	For CD-ROM
20	2	JP7,JP8	HEADER 3	Jumper with Shunt	For Selecting Lineout/ SPKR out
21	1	J1	LINEOUT PUT	Audio Jack	Line Out/ SPKR Out
22	1	J2	MIC	Audio Jack	Microphone Jack
23	1	J3	LINEINPU T	Audio Jack	Line input Jack

[1] Only Load FB3 or FB5 Depends on CODEC. Default FB3 Only

Item #	QTY	Reference	Part	Type/ Package	Comments/ Assembly
24	***1***	***L3***	***Bead***	***Axial***	***Load For Amplifier. Default No LOAD***
25a	15	R3,R4,R7,R20,R61,R74,R75 ,R76,R77,R78,R79, R80,R81,R98,R99	0	Resistor 1/10W SMD 0805 5%	
25b	***1***	***R2***	***0***	***Resistor 1/10W SMD 0805 5%***	***Load For Amplifier. Default No LOAD***
26	1	R13	4.7K	Resistor 1/10W SMD 0805 5%	
27	***2***	***R14,R16***	***15K***	***Resistor 1/10W SMD 0805 5%***	***Load For Amplifier. Default No LOAD***
28a	***2***	***R15,R17,***	***10K***	***Resistor 1/10W SMD 0805 5%***	***Load For Amplifier. Default No LOAD***
28b	8	R28,R64,R88,R89,R90, R91,*R100,R101*[2]	10K	Resistor 1/10W SMD 0805 5%	
29	***2***	***R18,R19***	***1.2K***	***Resistor 1/10W SMD 0805 5%***	***Load For Amplifier. Default No LOAD***
30	2	R27,R29	47	Resistor 1/10W SMD 0805 5%	
31	6	R49,R50,R53,R54,R57, R58	1K	Resistor 1/10W SMD 0805 5%	
32	1	R59	47K	Resistor 1/10W SMD 0805 5%	
33	2	R68,R71	25	Resistor 1/10W SMD 0805 5%	

[2] **R100,R101 required only for CODEC that Do Not Support VREFOUT. (Note These are not reflected in the current gerbers for Rev. B)**

Item #	QTY	Reference	Part	Type/ Package	Comments/ Assembly
34	5	R84,R85,R86,R87, R97	2.2K	Resistor 1/10W SMD 0805 5%	
35	1	U1	4DWAVE	100 pin LQFP	Trident Audio Chip
36	**1**	**U2**	**LT1587CM-3.3**	**Voltage Regulator**	**Do Not Load**
37	1	U2A	AME8613 3-UP	Voltage Regulator	Load
38	***1***	***U3***	***KA2206***	***Power Amp DIP***	***DO NOT LOAD***
39	1	U4	AC97#1	ADI 1819A	AC97 CODEC Trident Approved
40	1	Y2	24.576MHz	Cardinal Crystal	

NOTE:

All Items in BOLD and Italics are components associated with Power Amplifier. We do not recommend populating these.