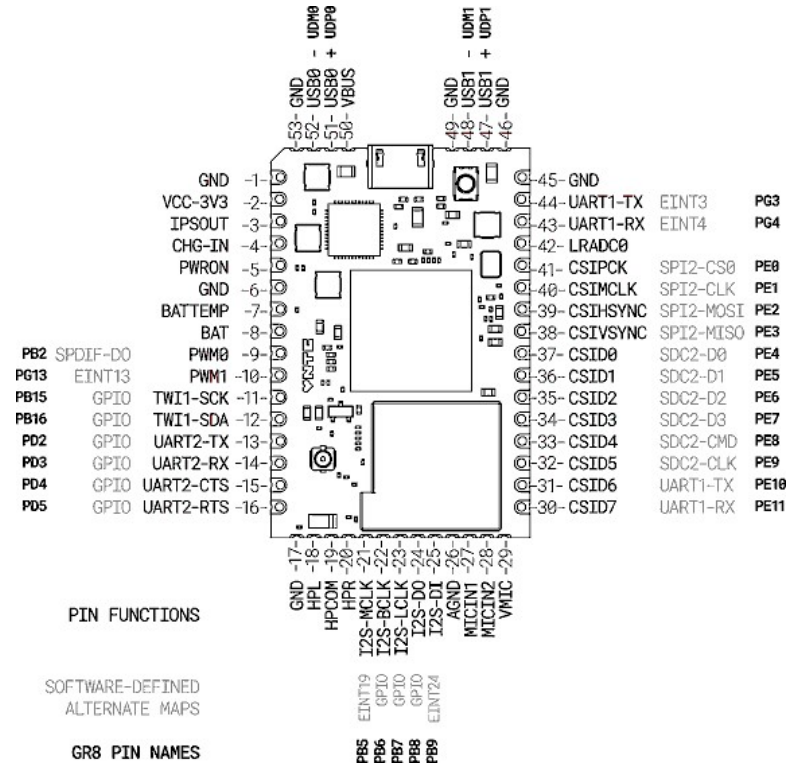


REVISION HISTORY

Schematics Index:

- P01: REVISION HISTORY
- P02: BLOCK
- P03: CPU
- P04: POWER
- P05: MISC
- P06: SDIO WIFI
- P07: USB
- P08: BESIDE CPU
- P09: NAND



Revision History	Description	Date	Drawn	Checked	Changelist
CHIP Pro	version 0.1	2016-08-05			
CHIP Pro	version 0.9	2016-11-11			
CHIP Pro	version 0.9a	2017-03-01			fix sheet 1 pinout dwg
CHIP Pro	version 1.0	2017-03-31			FCC/CE/IC Certification

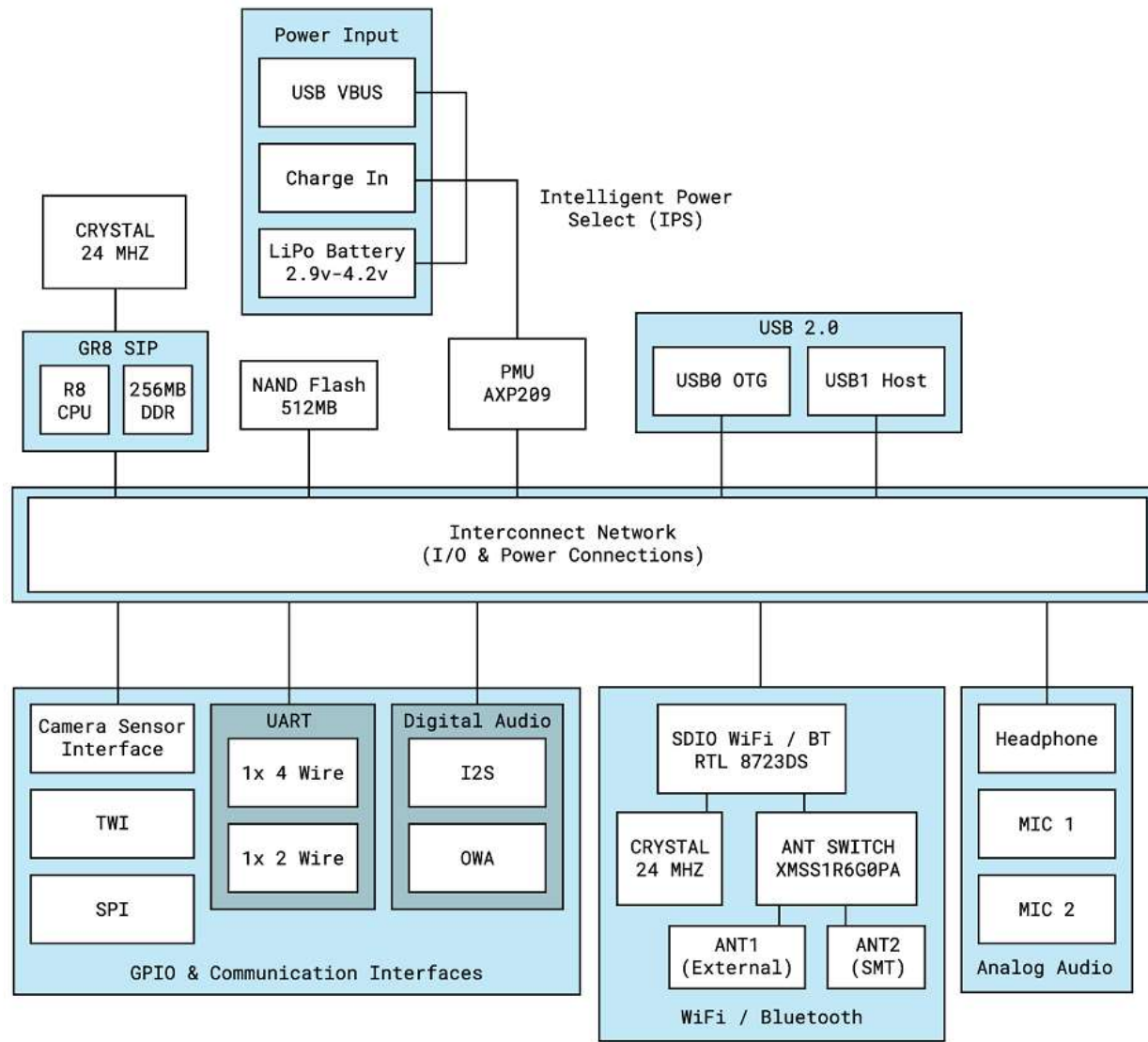
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BLOCK



TP list	Function
TP 0	FEL
TP 1	USB0-ID
TP 2	USB0-D+
TP 3	USB0-D-
TP 4	TWI0-SDA
TP 5	TWI0-SCK
TP 6	DC3-SET

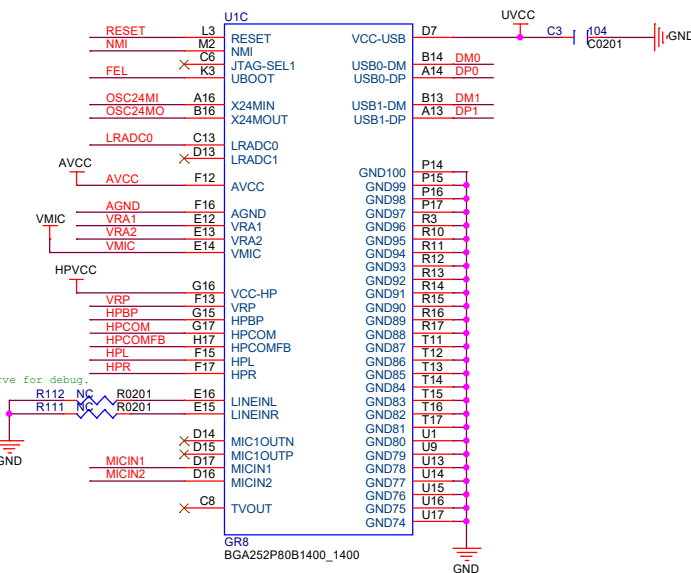
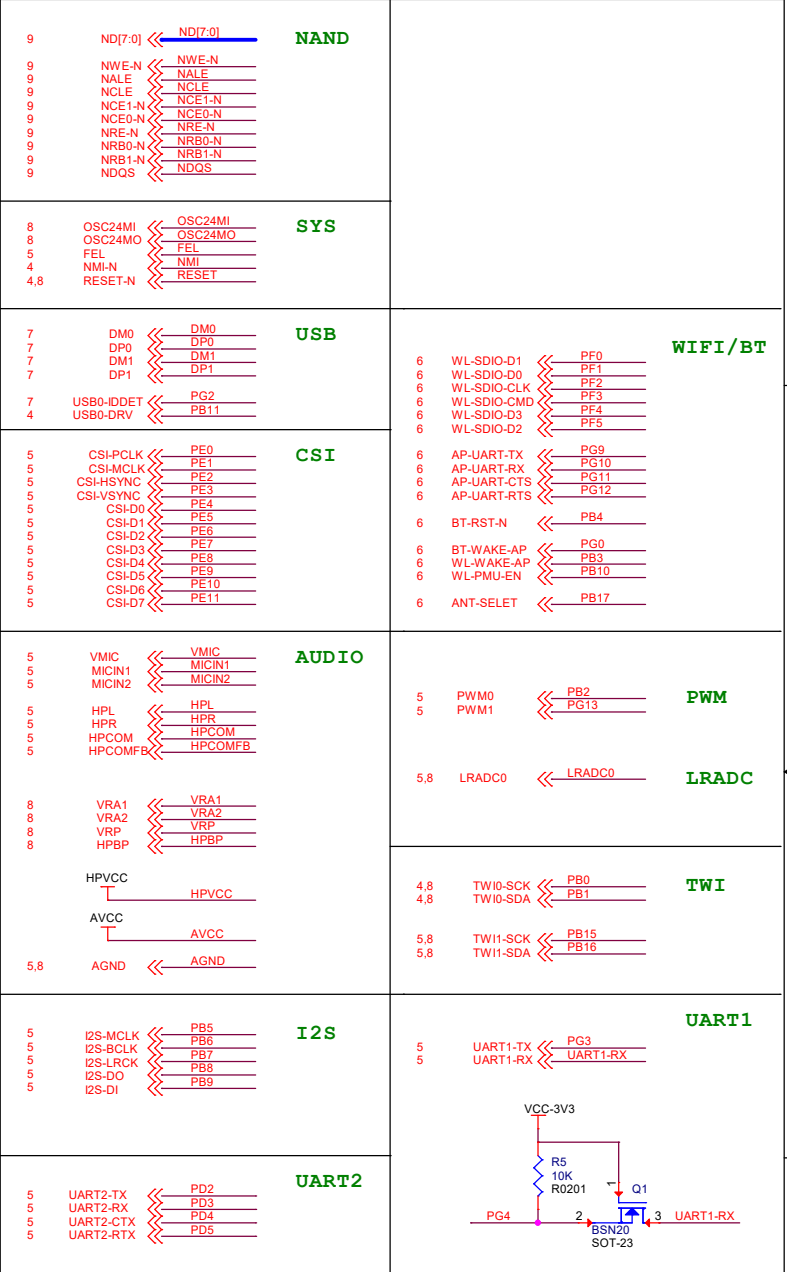
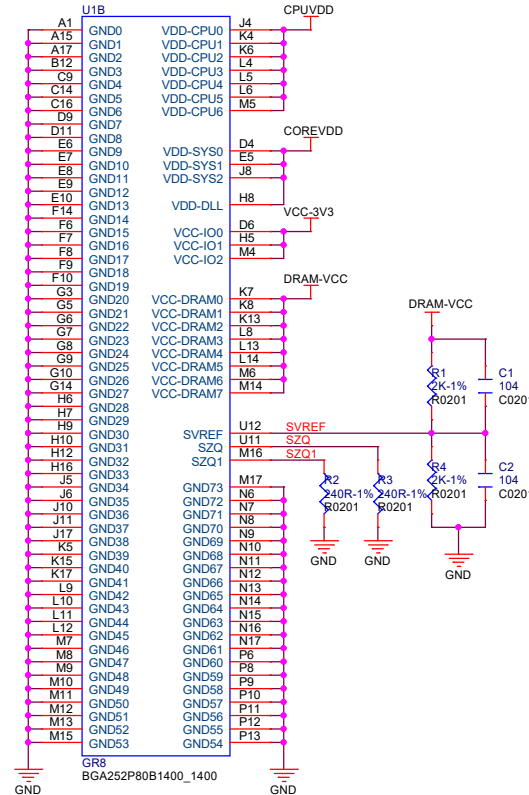
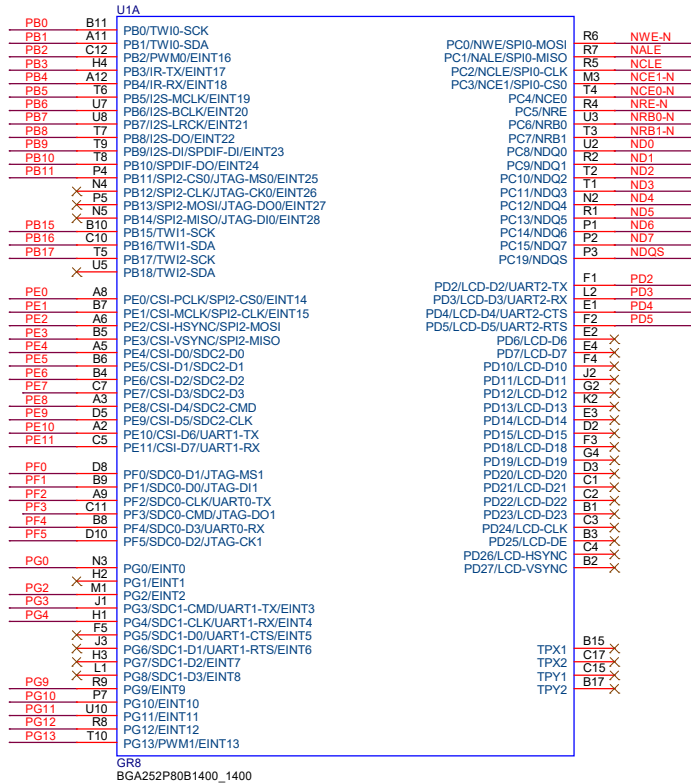
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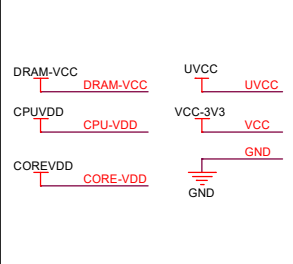
CPU



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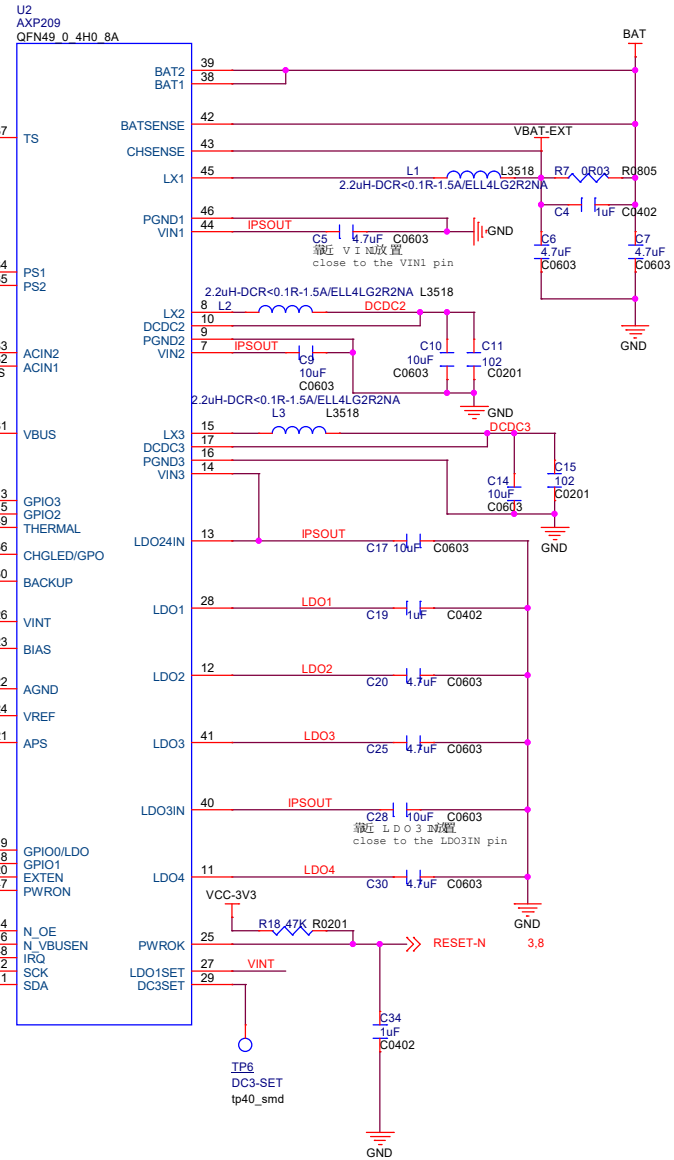
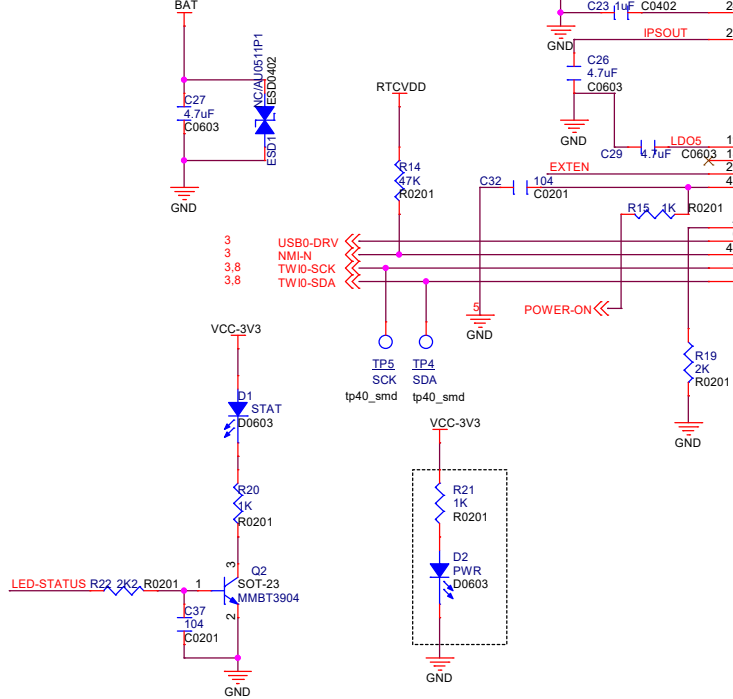
Design Name		C.H.I.P. Pro	
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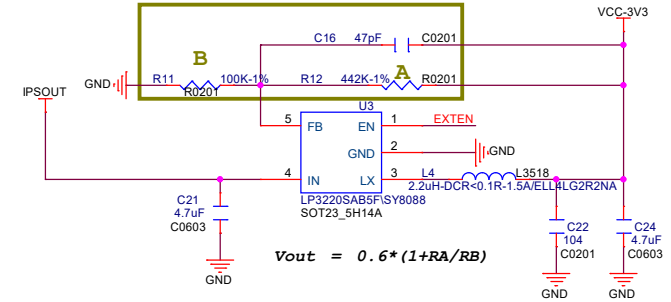
POWER/PMU

CPUVDD	DCDC2	MAX 1200MA
COREVDD	DCDC3	MAX 1600MA
RTCVDD	LDO1	MAX 200MA
AVCC	LDO2	MAX 200MA
LDO3	LDO3	MAX 200MA
LDO4	LDO4	MAX 200MA
VCC-1V8	LDO5	MAX NC/50MA
VCC-3V3	VCC-3V3	MAX 1000MA
DRAM-VCC	DRAM-VCC	MAX 1000MA

BATTERY IN

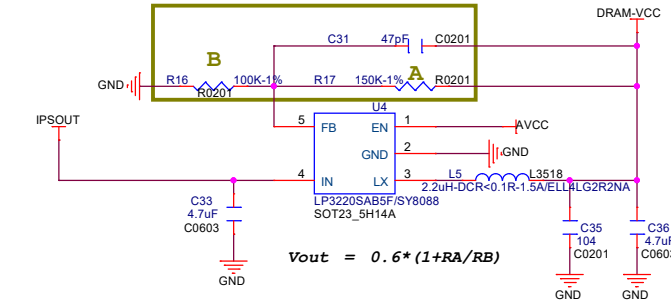


IPSOUT TO 3V3



$$V_{out} = 0.6 * (1 + RA/RB)$$

IPSOUT TO 1V6



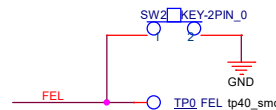
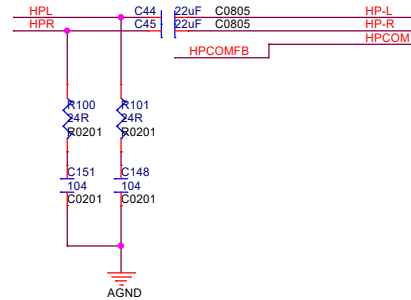
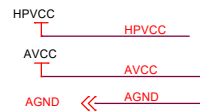
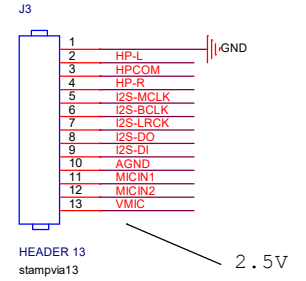
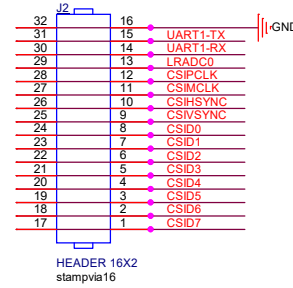
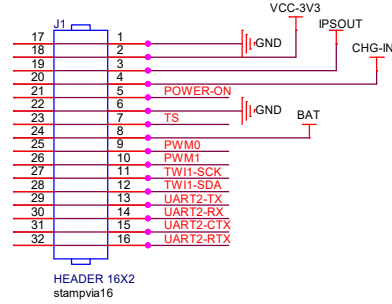
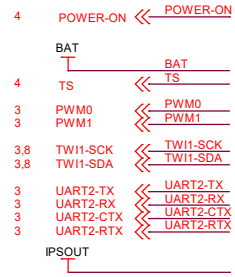
$$V_{out} = 0.6 * (1 + RA/RB)$$

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MISC



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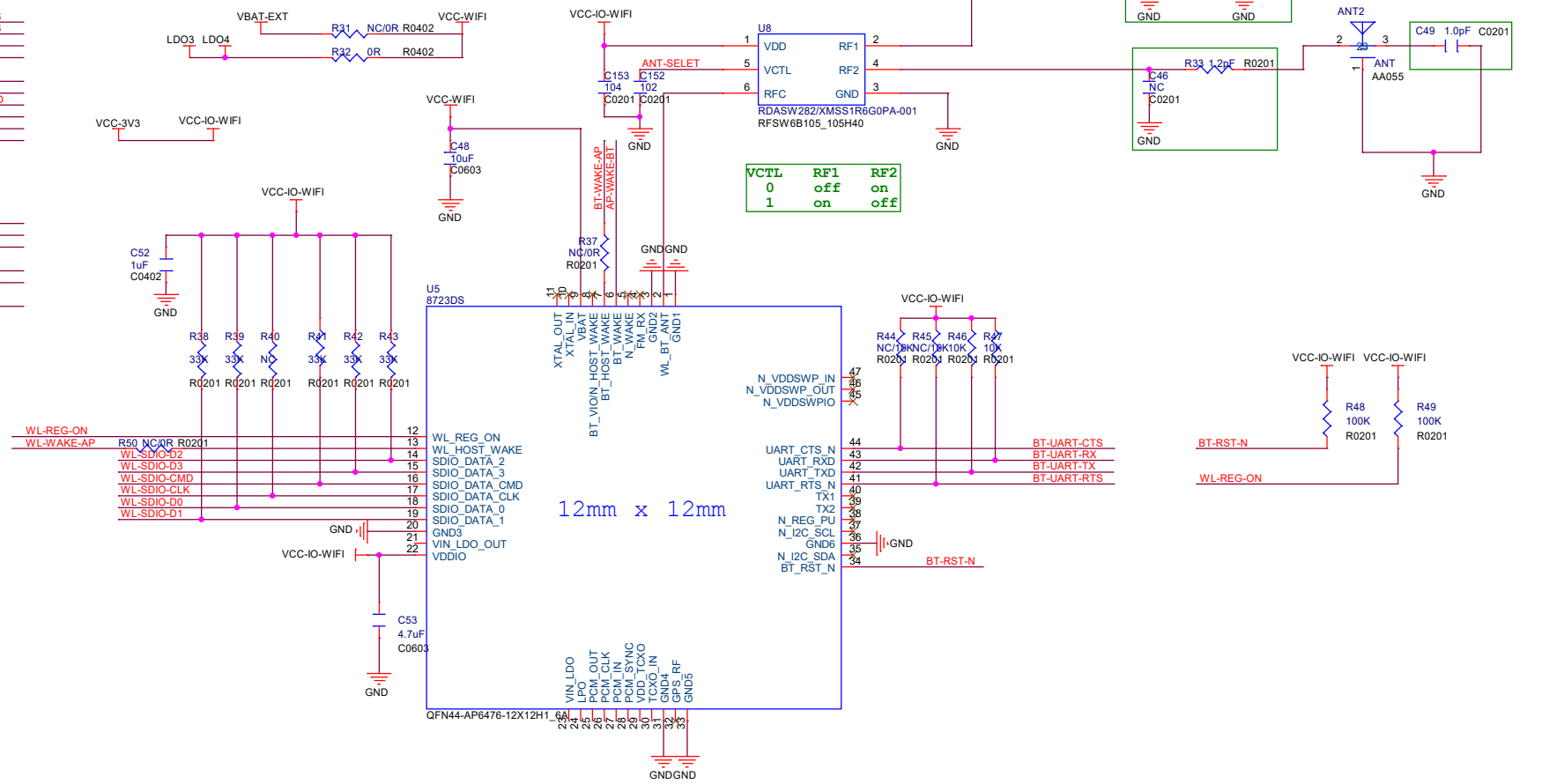
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SDIO WIFI&BT

- 3 AP-UART-CTS << BT-UART-RTS
- 3 AP-UART-RTS << BT-UART-CTS
- 3 AP-UART-RX << BT-UART-TX
- 3 AP-UART-TX << BT-UART-RX

- 3 WL-PMU-EN << WL-REG-ON
- 3 BT-RST-N << BT-RST-N
- 4 AP-WAKE-BT << AP-WAKE-BT
- 3 BT-WAKE-AP << BT-WAKE-AP
- 3 WL-WAKE-AP << WL-WAKE-AP
- 3 ANT-SELET << ANT-SELET



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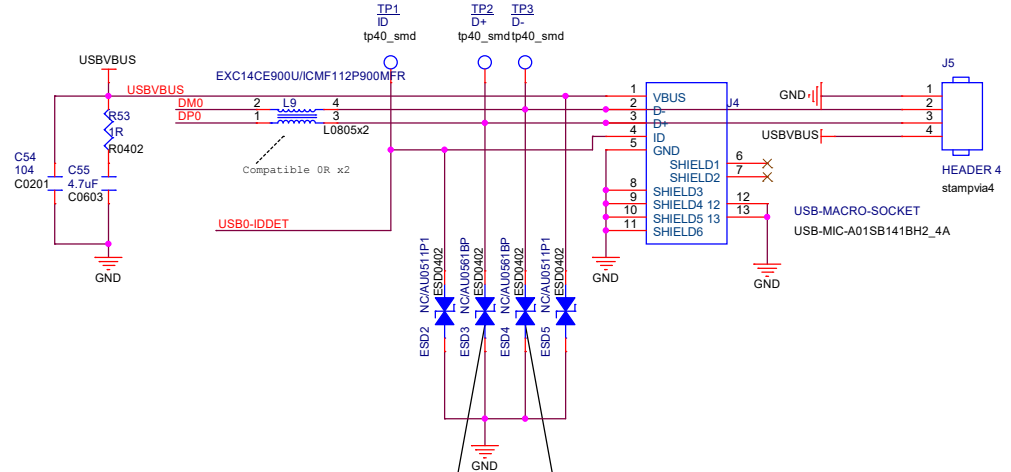
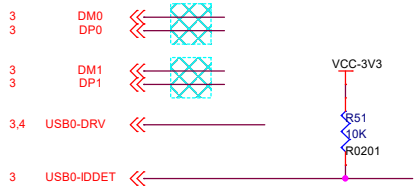
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USB



D+ / D- 上的 ESD 电容 小于等于 4pF (考虑误差)。
 The parasitic capacitance of esd on D+/D- < 4pF



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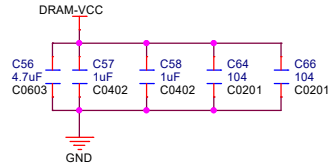
Design Name: **C.H.I.P. Pro**

Size: A3	Page Name: USB	Rev: v1.0
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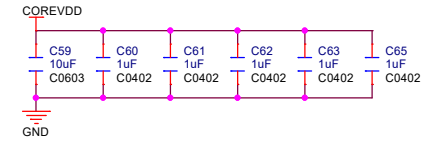
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BESIDE CPU

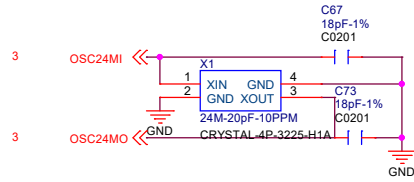
DRAM



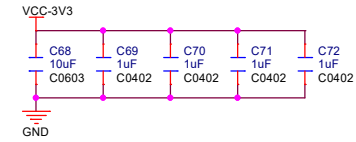
CORE



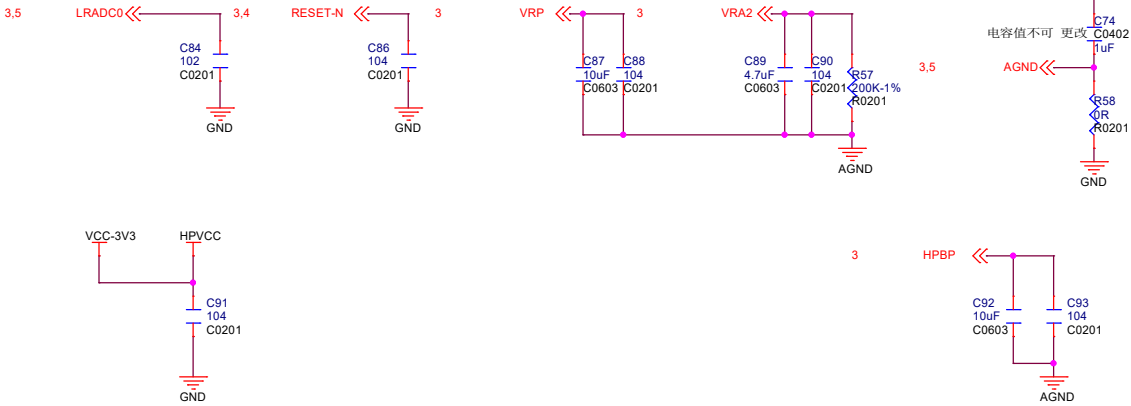
CRYSTAL



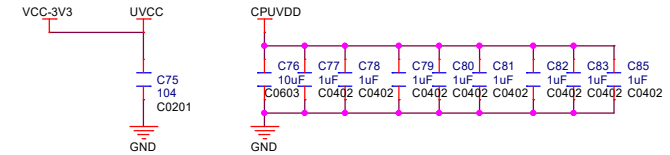
PIO-INTERFACE



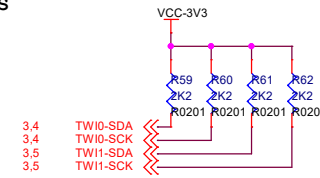
AUDIO-TP



USB-CPU



OTHERS

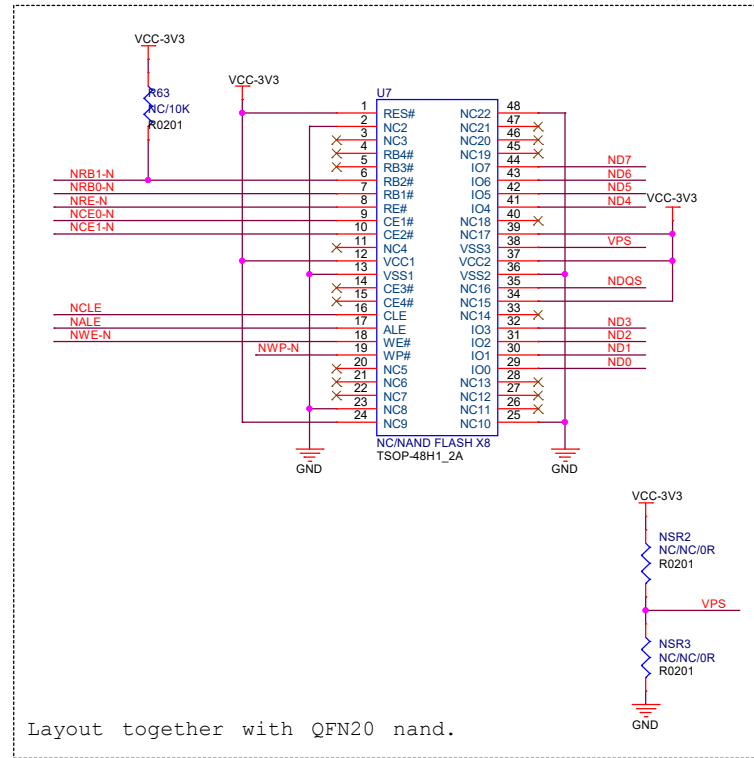
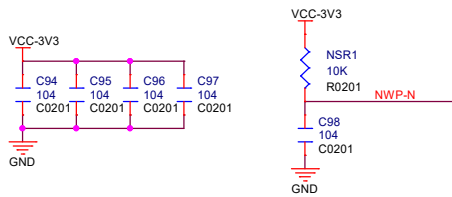
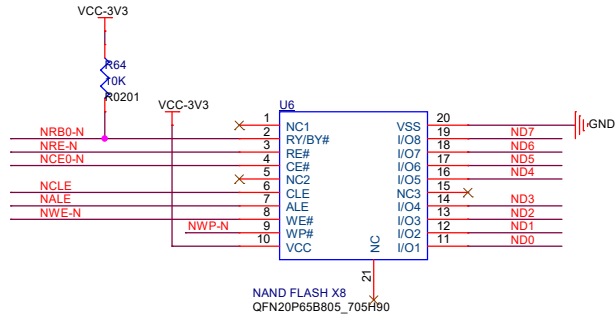
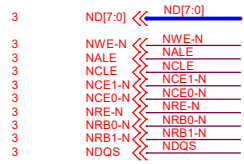


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NAND



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